Welcome To

ISSCC 2014
Session 8
Optical Links and Copper PHYs

A 6Gb/s Transceiver with a Nonlinear Electronic Dispersion Compensator for Directly Modulated Distributed-Feedback Lasers

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KAIST

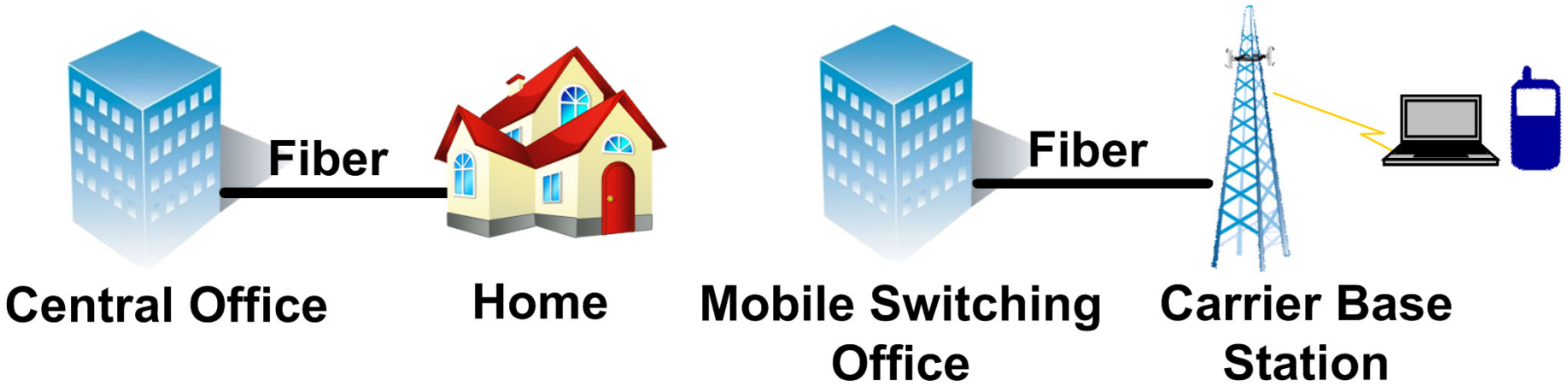
NANOSCALE ADVANCED
INTEGRATED SYSTEMS LAB

Outline

- **Introduction and Background**
  - Chirp-induced dispersion from directly modulated laser
  - Solution : Nonlinear electronic dispersion compensator (EDC)
- **Proposed EDC technique**
  - TX pre-compensation: Pre-emphasis and pulse-width control
  - RX post-compensation: Linear and nonlinear equalization
- **Measurement results**
- **Conclusions**

Motivation

- Fiber to the x (FTTx) is growing fast.
  ex) Fiber to the home (FTTH), LTE backhaul

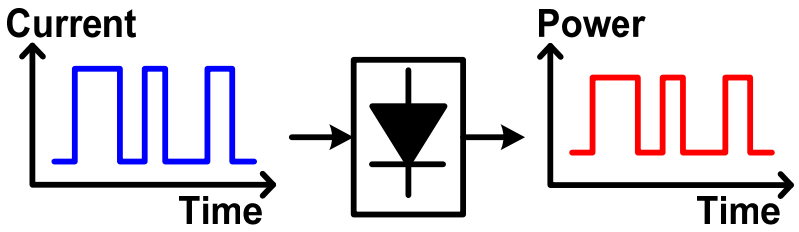


- To reduce cost per subscriber

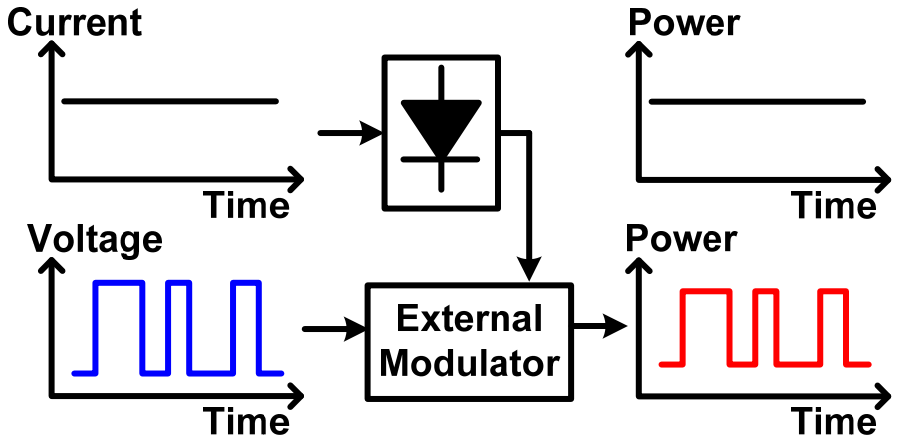
→ **Cost-effective laser module** is demanded.

Motivation

- **Directly Modulated Laser (DML)**
  - Low cost and power
  - Compact size
  - Frequency Chirp
    (> 20km @ 6Gb/s)



- **Externally Modulated Laser (EML)**
  - High performance
  - High cost and power
  - External modulator



Solutions

Previous approach

- **Optical Domain Solution**
  - Chirp-managed laser (CML) with an optical spectrum reshape (OSR) filter
  - Dispersion compensation fiber (DCF)

    → Expensive and impractical solution

This work

- **The First Electrical Domain Solution**
  - Analog domain nonlinear EDC

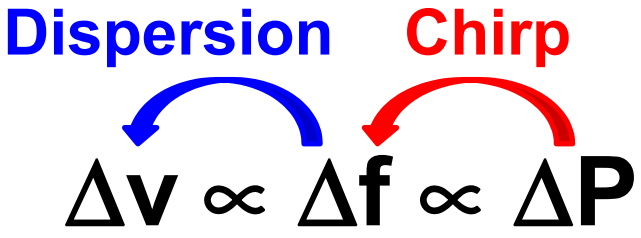
Frequency Chirp

Chirp

- Frequency increases in proportion to the power

Interaction with chromatic dispersion

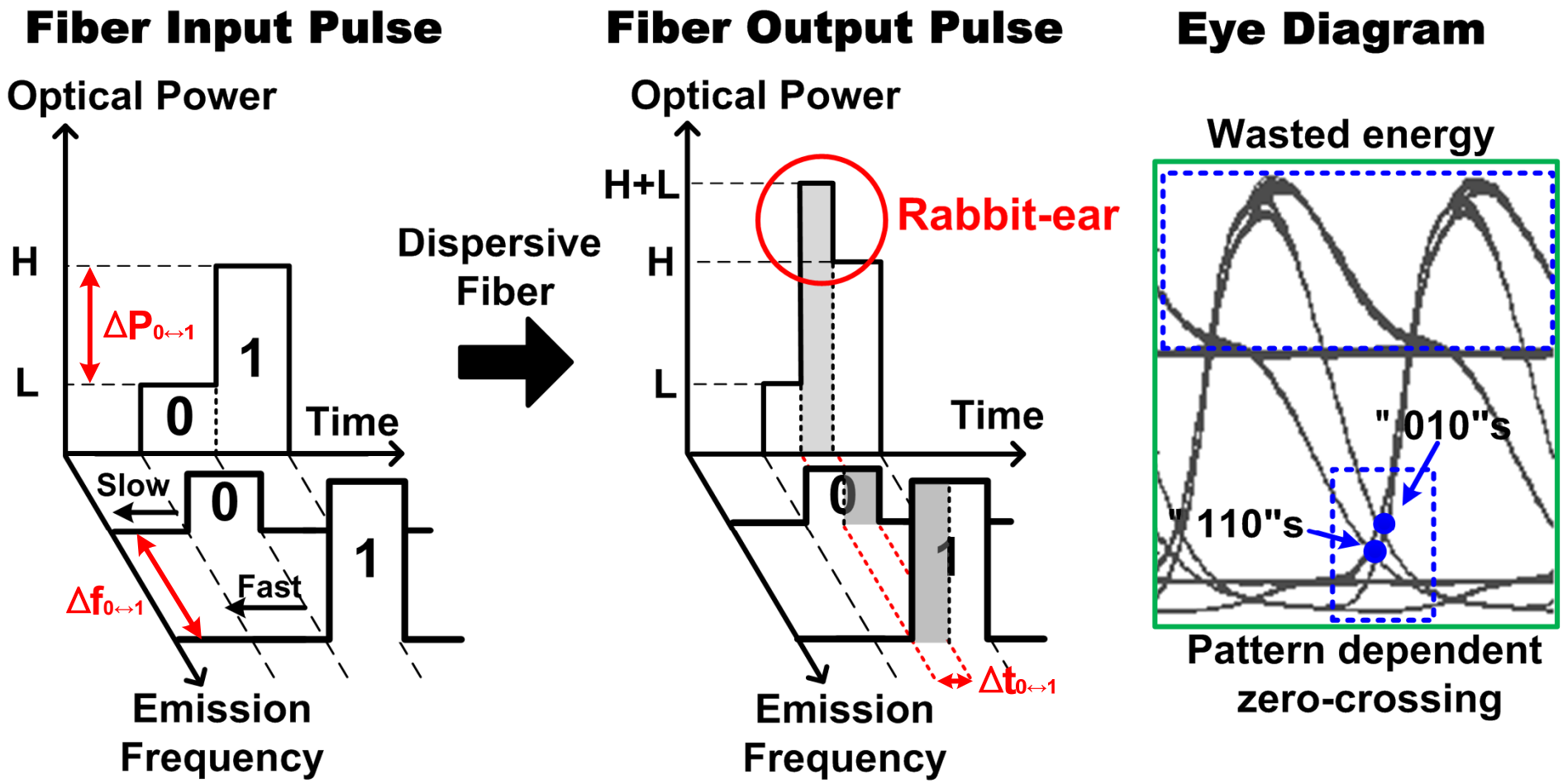
- Wave velocity increases in proportion to the emission frequency.



→ **High power signal propagates faster**

Linear Chirp-dispersion

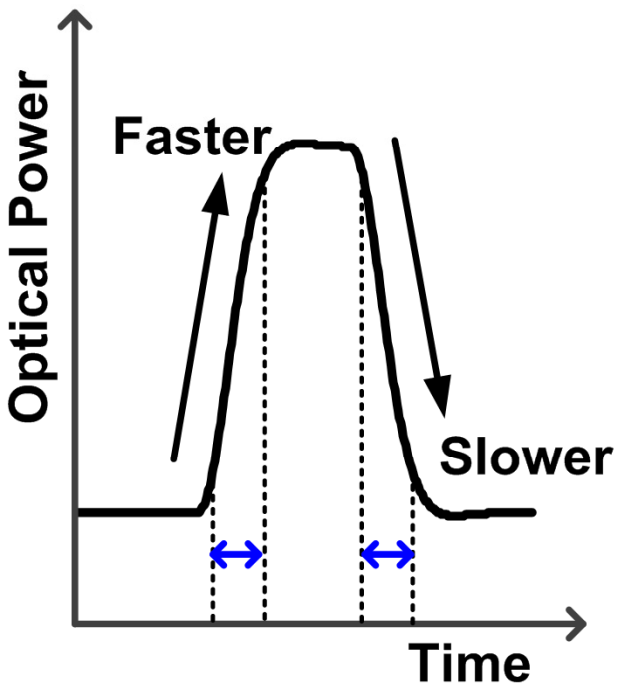
Rabbit-ear effect



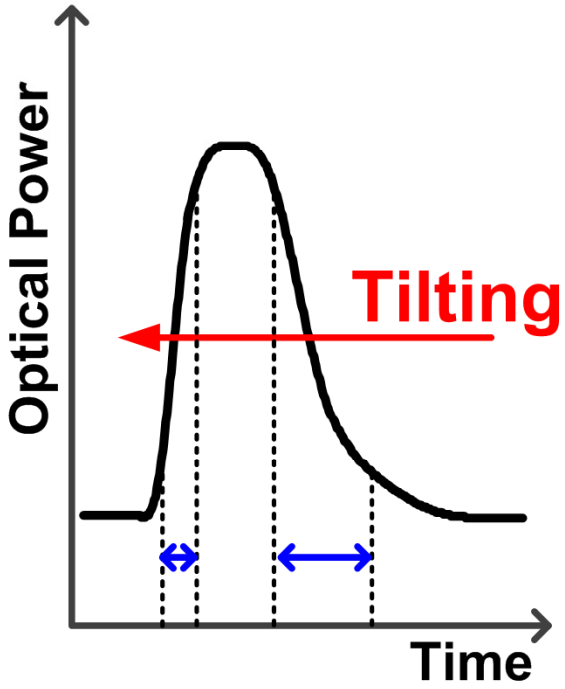
Nonlinear Chirp-dispersion

Tilting effect

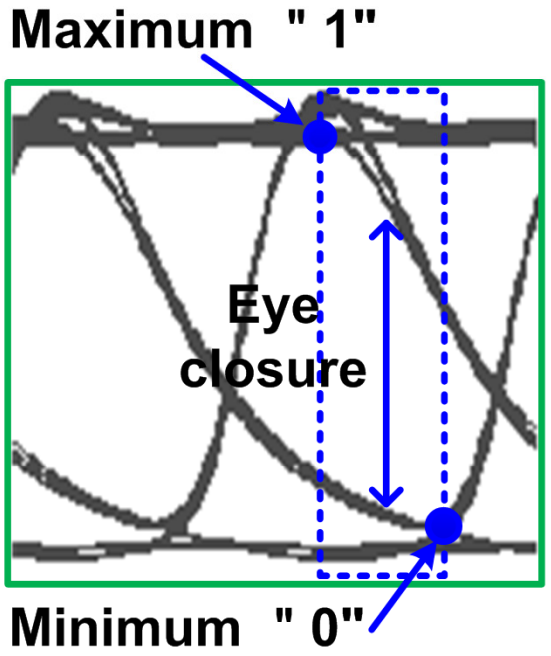
Fiber Input Pulse



Fiber Output Pulse

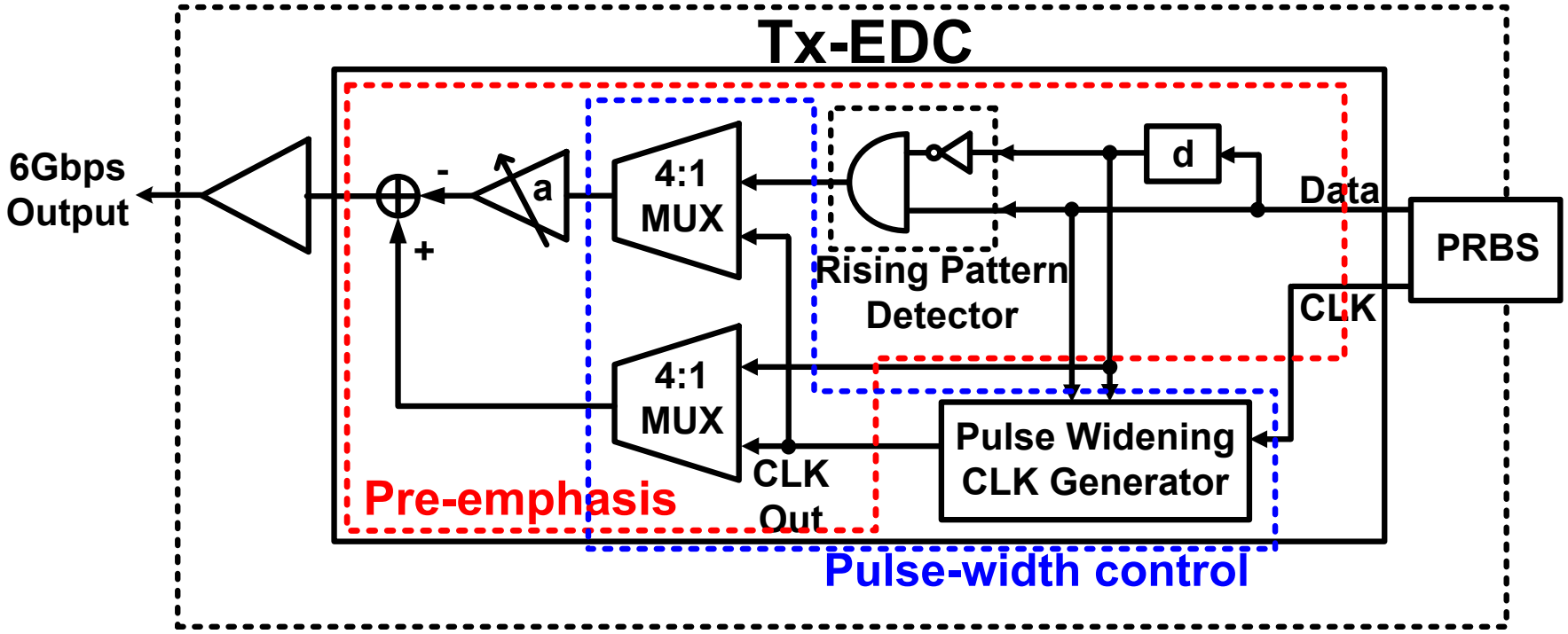


Eye Diagram



Transmitter-side EDC

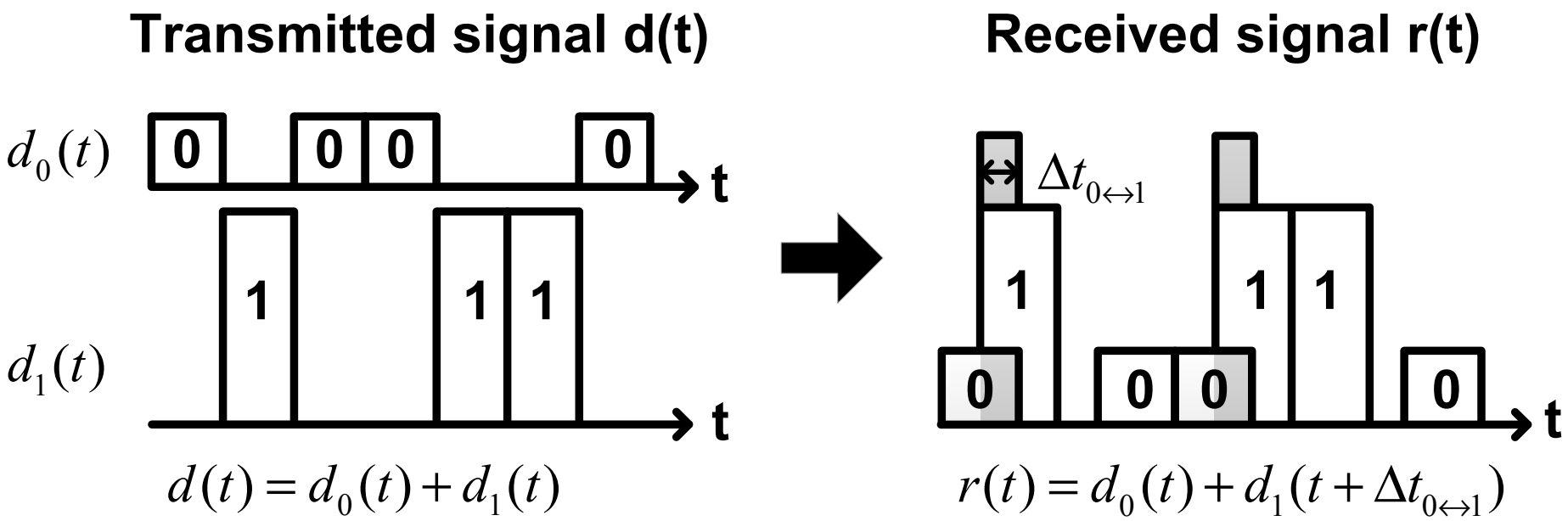
Overall architecture and features



- Pre-emphasis → Rabbit-ear reduction
- Pulse-width control → Duty-cycle distortion

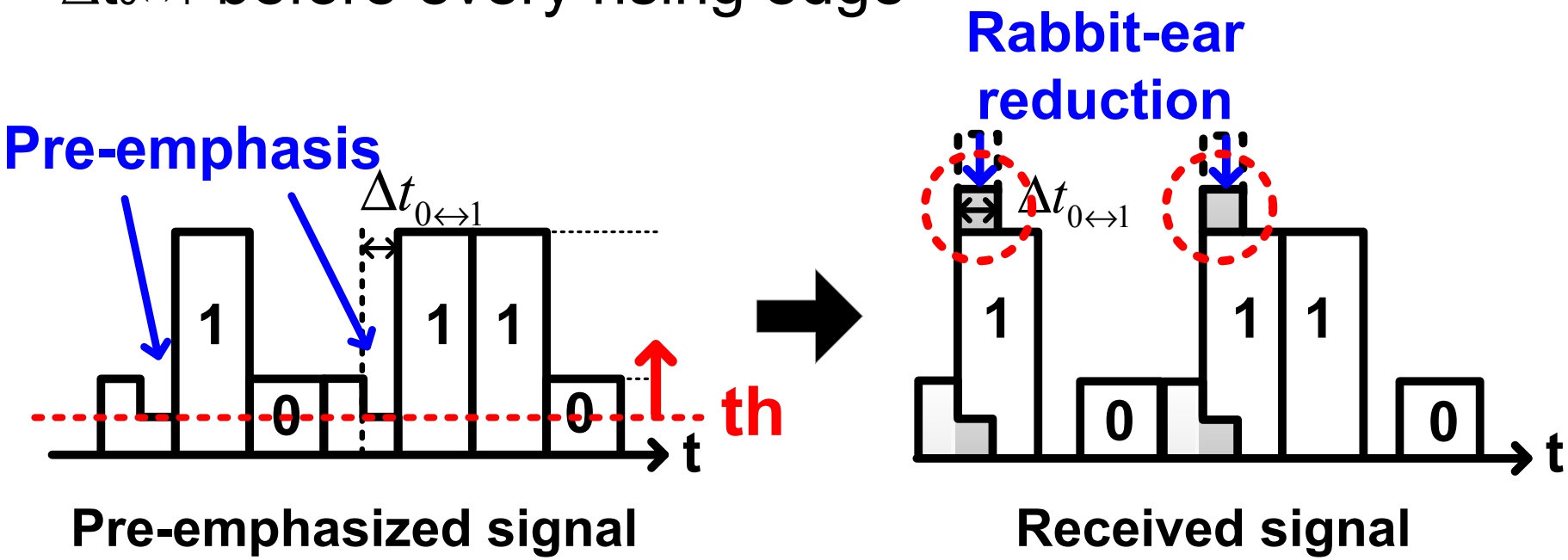
Rabbit-ear model

- Rabbit-ear appears during $\Delta t_{0\leftrightarrow 1}$ in every rising edge → Pattern-dependency



Pattern-dependent Pre-emphasis

- **Rabbit-ear reduction :** pre-emphasis $d_0(t)$ during $\Delta t_{0\leftrightarrow1}$ before every rising edge

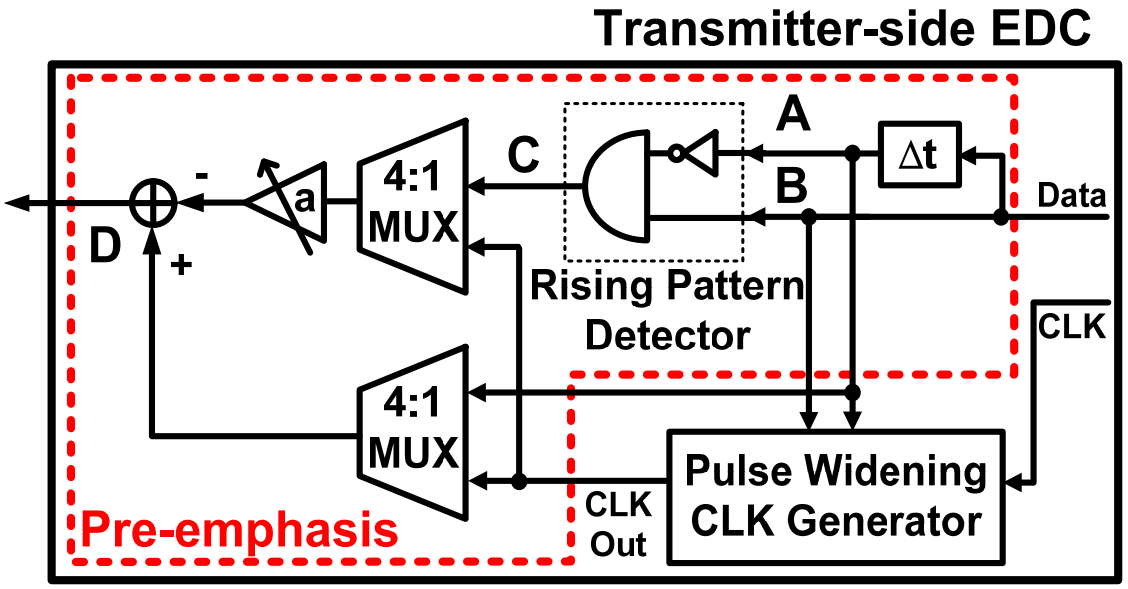


- **Limitation** : pre-emphasis limited by laser threshold

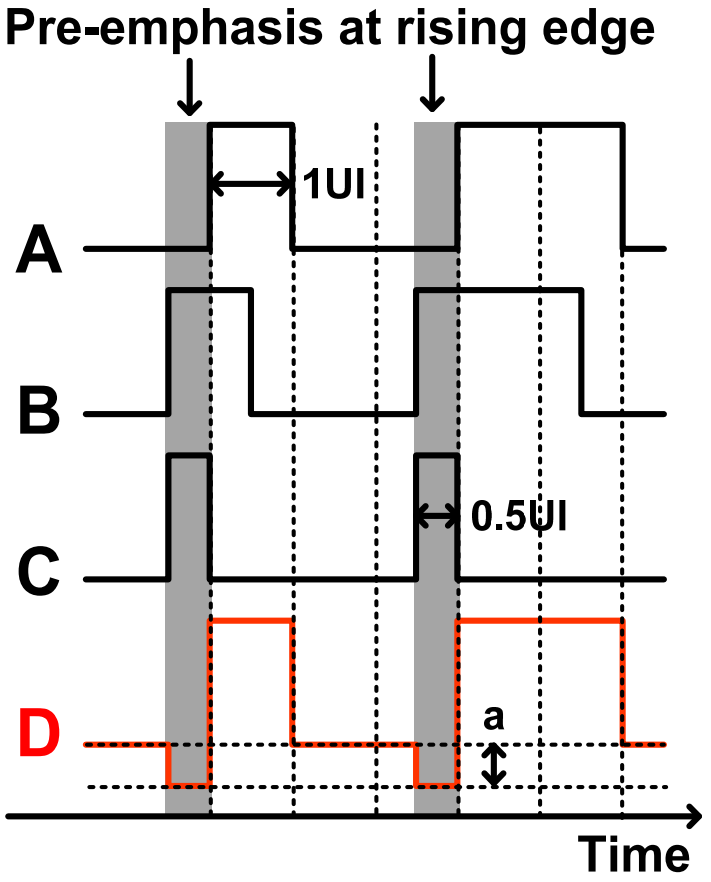
→ We need receiver-side solution

Pattern-dependent Pre-emphasis

Tx-EDC solution for rabbit-ear reduction

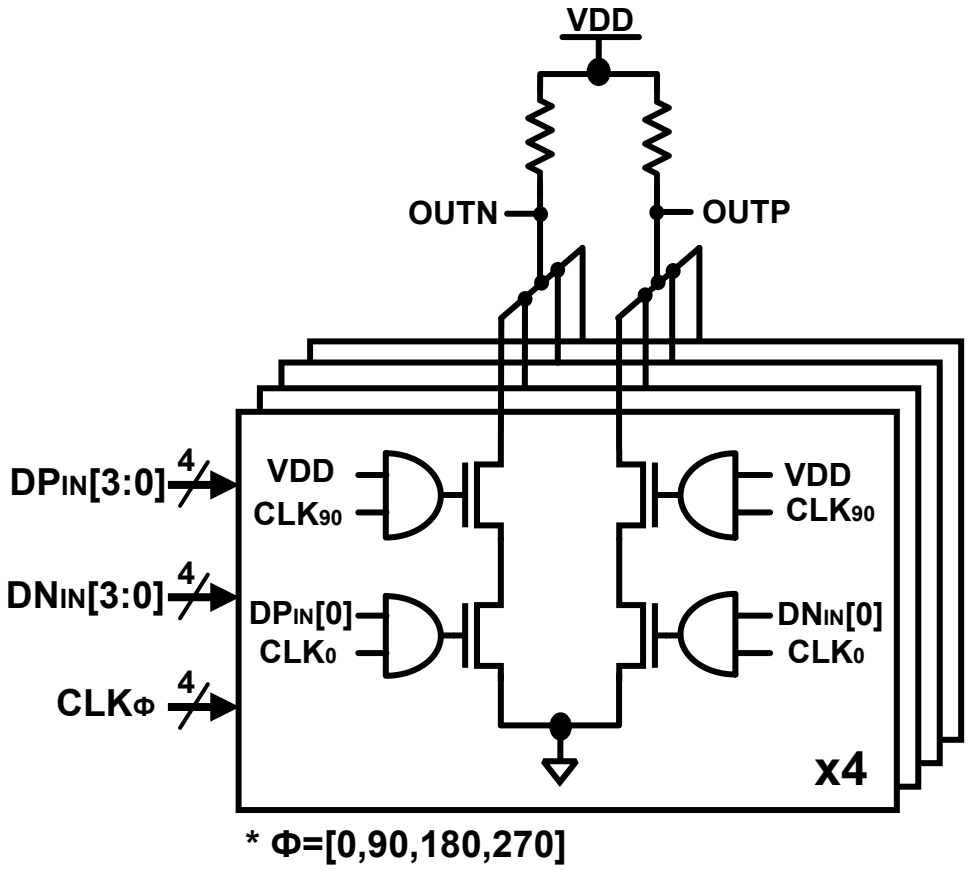


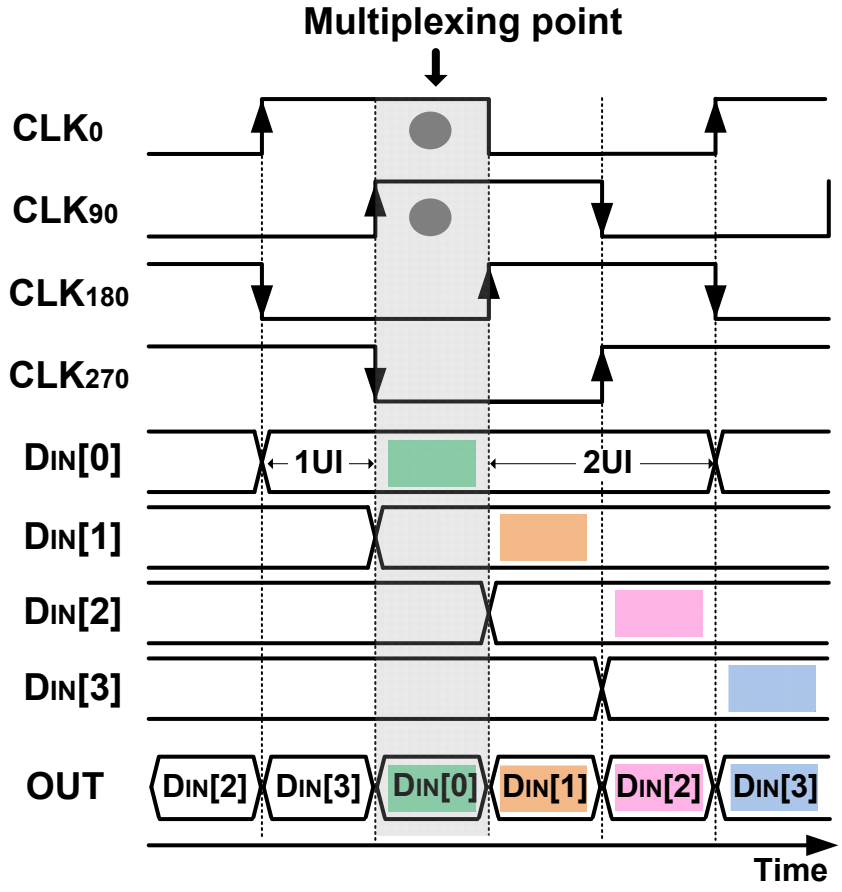
A : Main-tap data
B : Pre-tap data
C : Adjustment signal
D : Pre-emphasized signal



4:1 MUX for Pulse-width Control

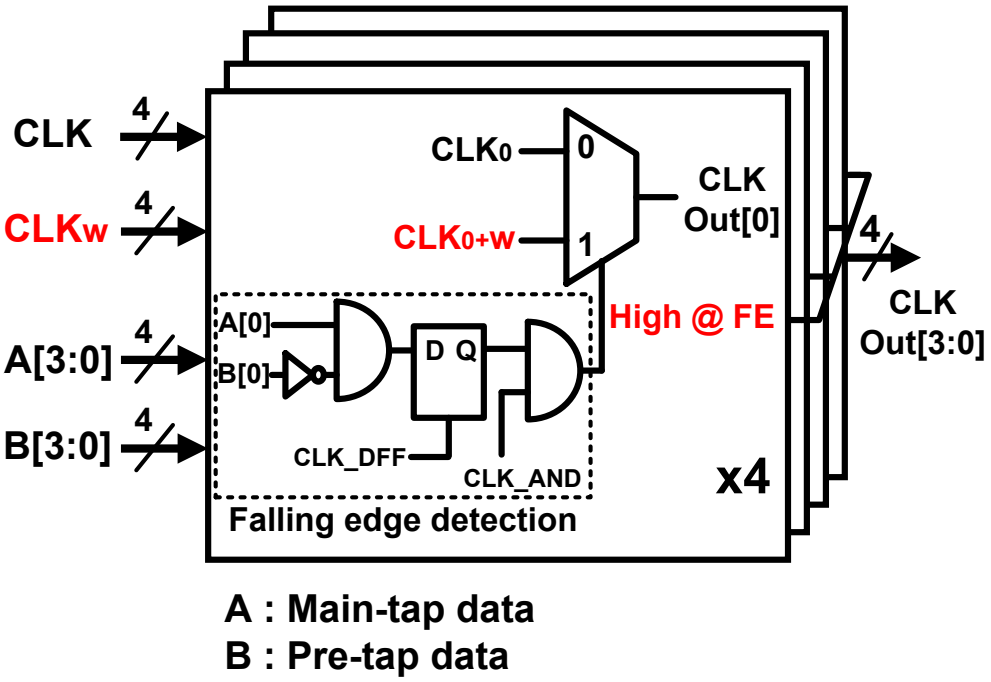
- Proper data path is selected through CLK overlaps

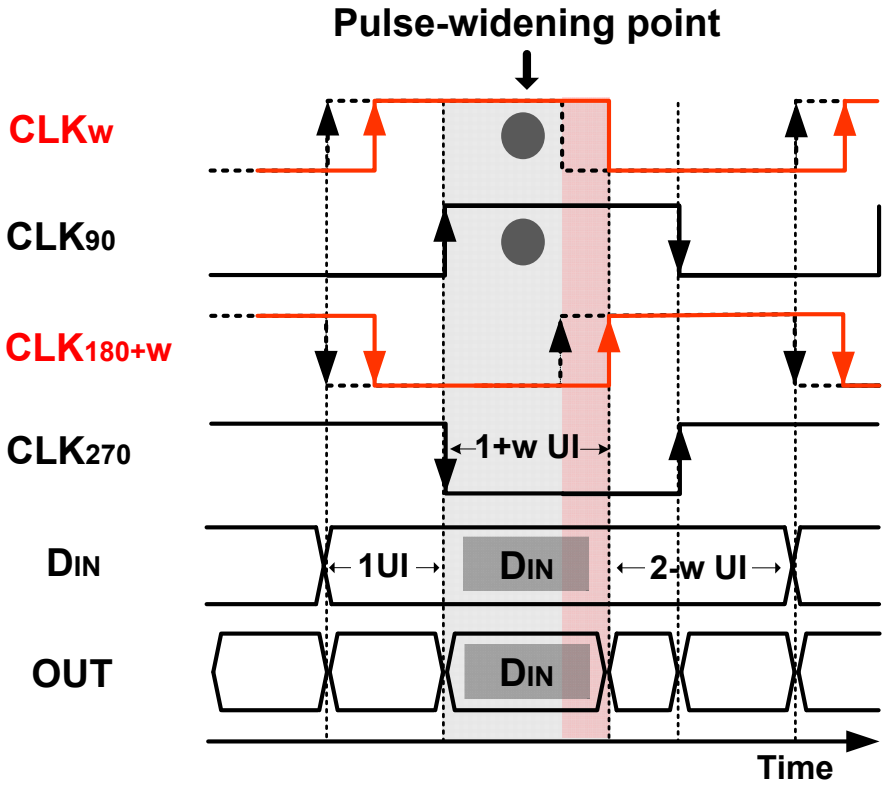




Pulse-widening CLK Generator

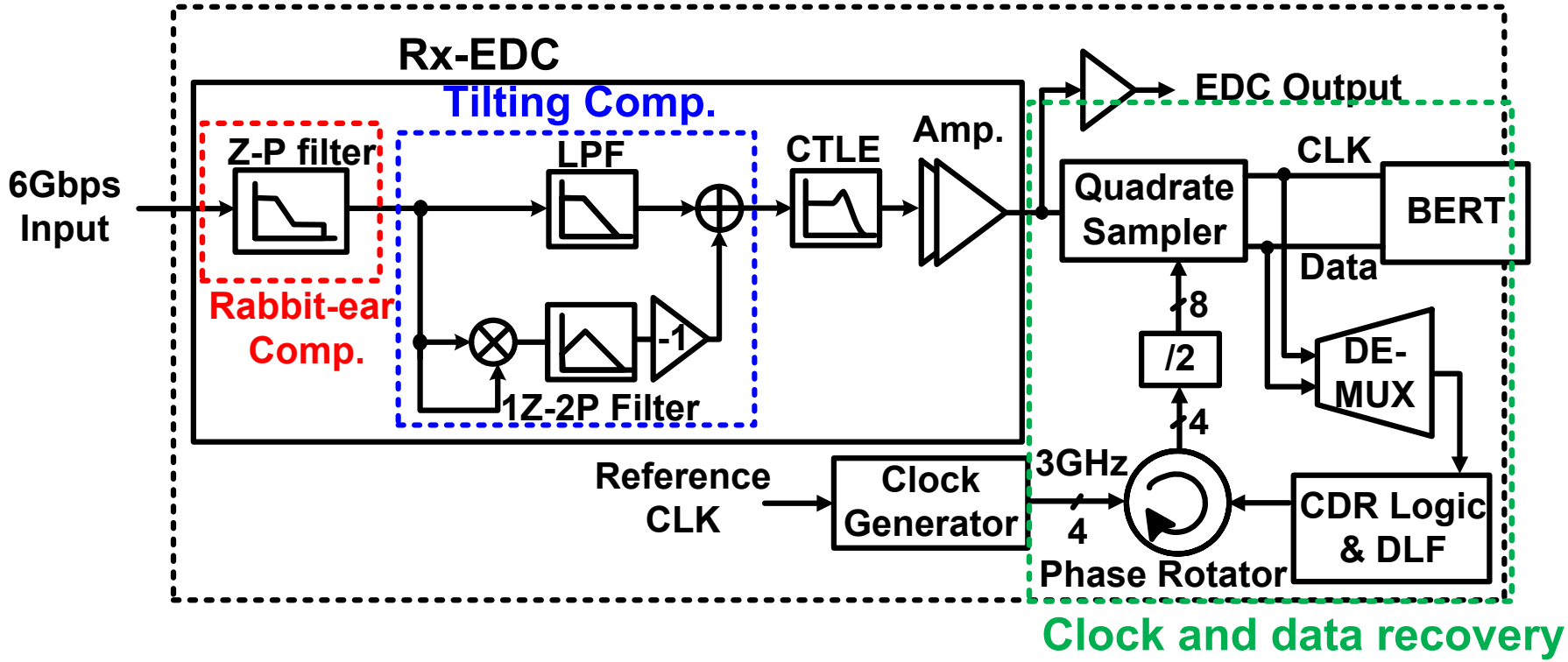
- At falling edge, a phase-shifted CLK is chosen
- W is programmable via phase interpolator (PI)





Receiver-side EDC

Overall architecture and features



- Linear filter → Rabbit-ear elimination
- Nonlinear equalizer → Tilting mitigation

Linear Filter for Rabbit-ear Elimination

Transfer function derivation

$$r(t) = d_0(t) + d_1(t + \Delta t_{0\leftrightarrow 1})$$

$$d(t) = d_0(t) + d_1(t)$$

$$r(t) = \frac{1}{ER - 1}\left[ER \cdot d(t + \Delta t_{0\leftrightarrow 1}) - d(t)\right]$$

Backward substitution

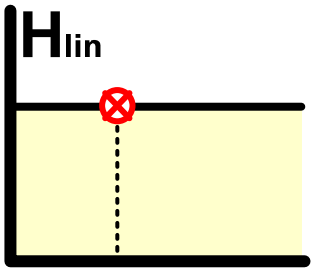
$$d(t) = \left(1 - \frac{1}{ER}\right)\left[r(t) + \frac{1}{ER} r(t - \Delta t_{0\leftrightarrow 1})\right]$$

$$\because ER^2 >> 1$$

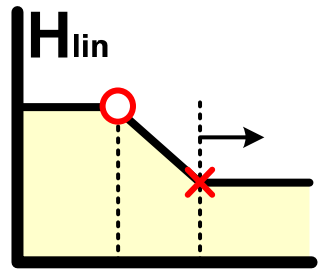
Taylor series

$$H_{lin} = \frac{D(s)}{R(s)} = \left(1 - \frac{2}{ER}\right)\frac{s + \frac{ER+1}{ER-1} \cdot p_{LF}}{s + p_{LF}}$$

i) ER→ ∞

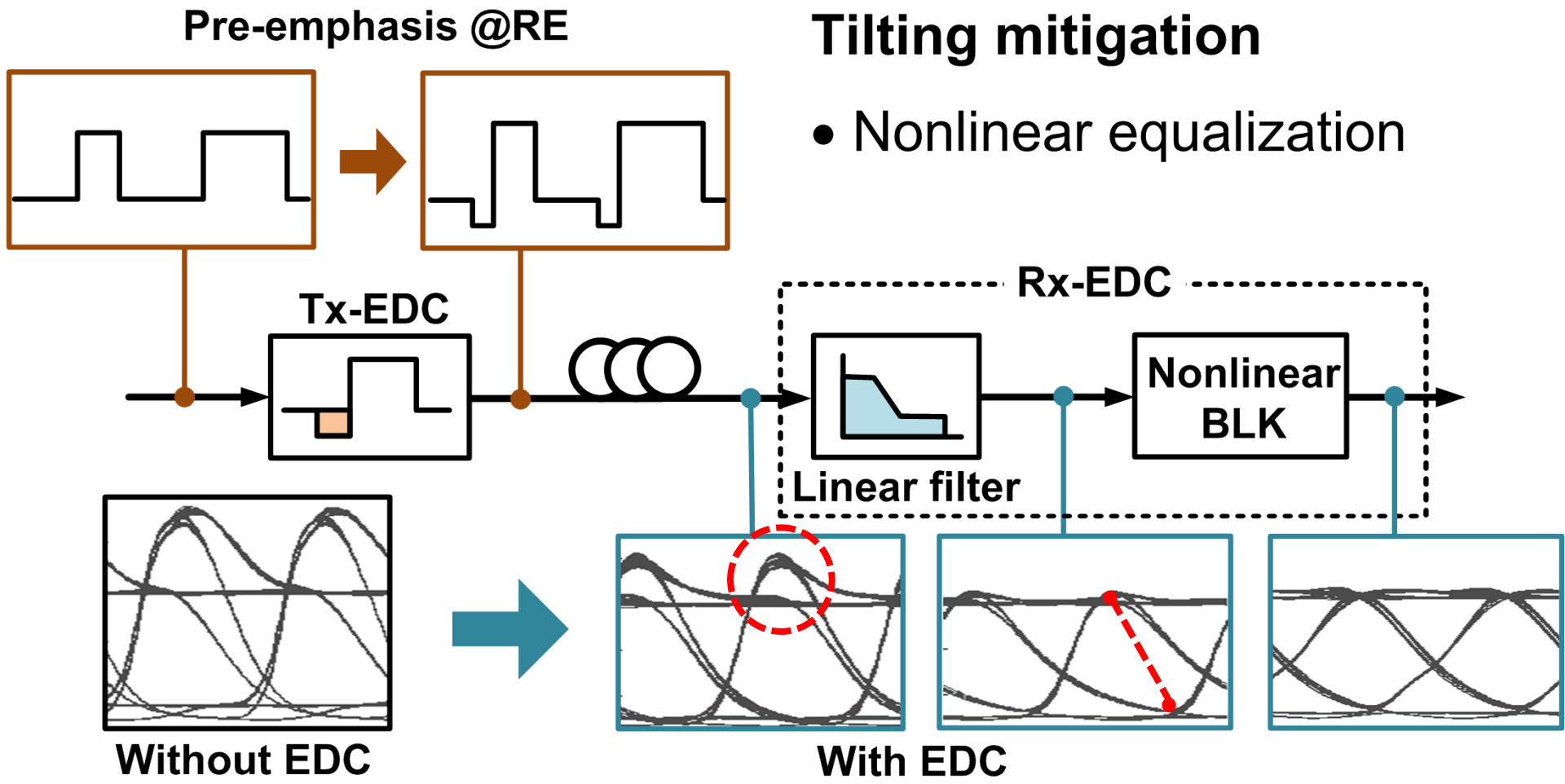


ii) ER↓



Typical

Rabbit-ear Elimination



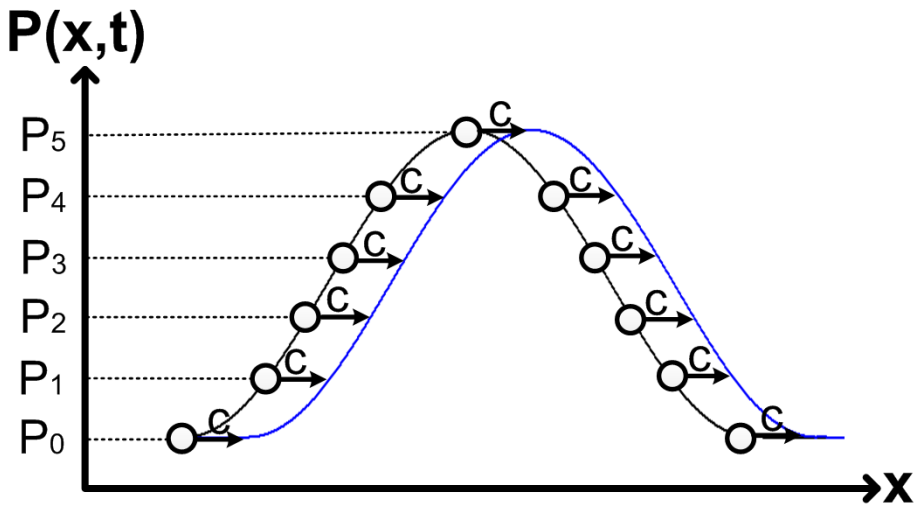
Tilting Modeling

The 1st order wave equation

- P(x,t) : power
- v(x,t)= c

$$\frac{dP}{dt} + c\frac{dP}{dx} = 0$$

Propagation speed

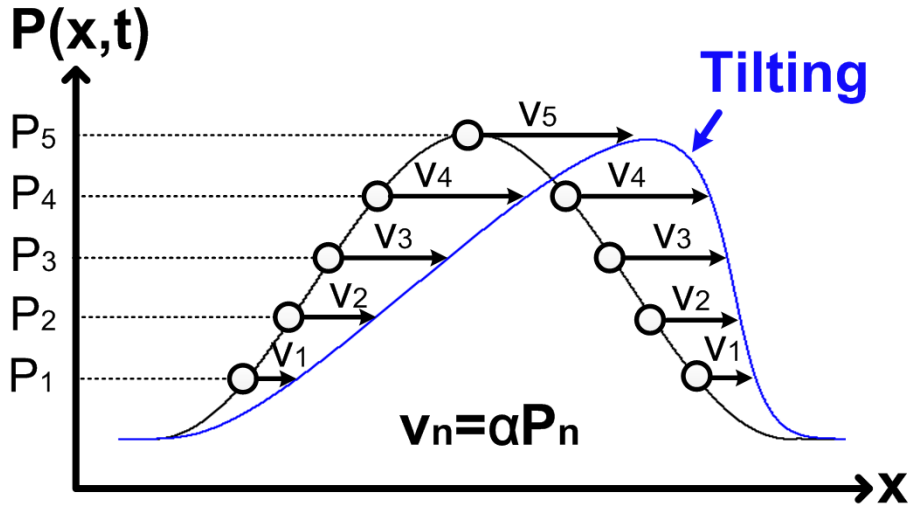


Burger's equation

- P(x,t) : power
- v(x,t) = αP(x,t)

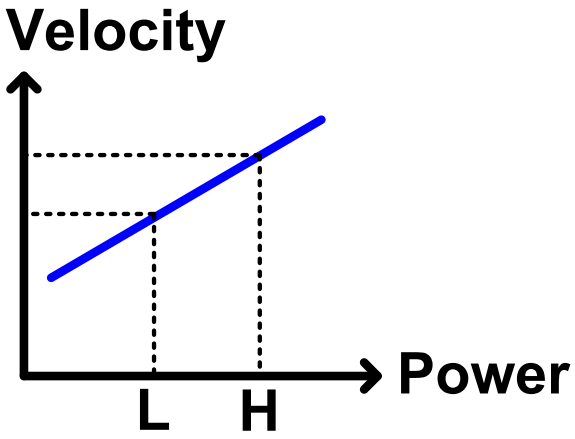
$$\frac{dP}{dt} + \alpha P\frac{dP}{dx} = 0$$

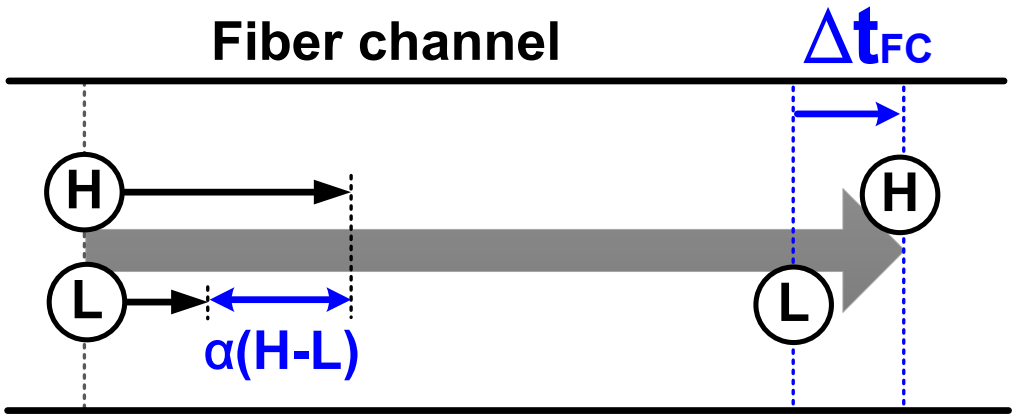
Propagation speed



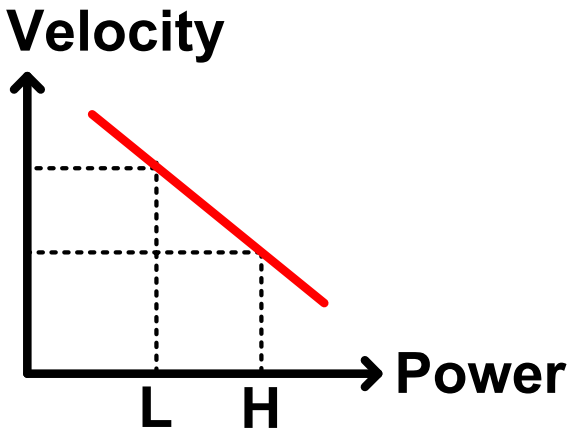
Tilting Compensation

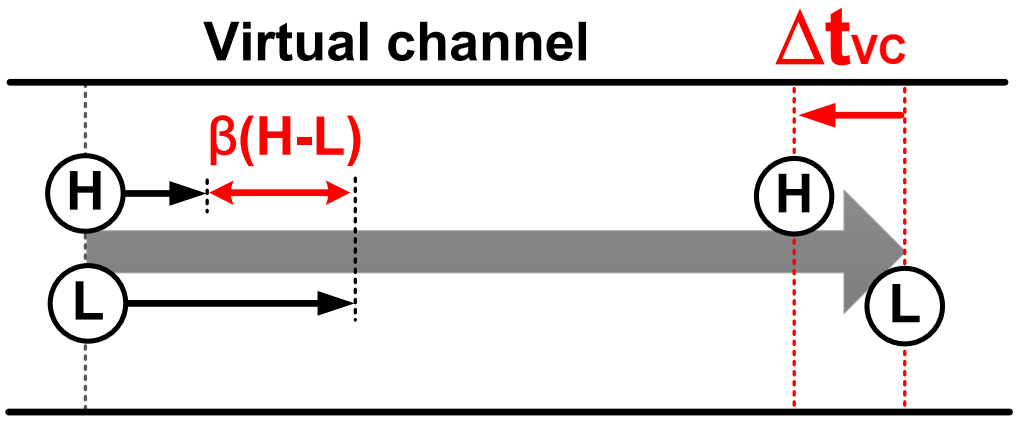
- **Fiber channel**





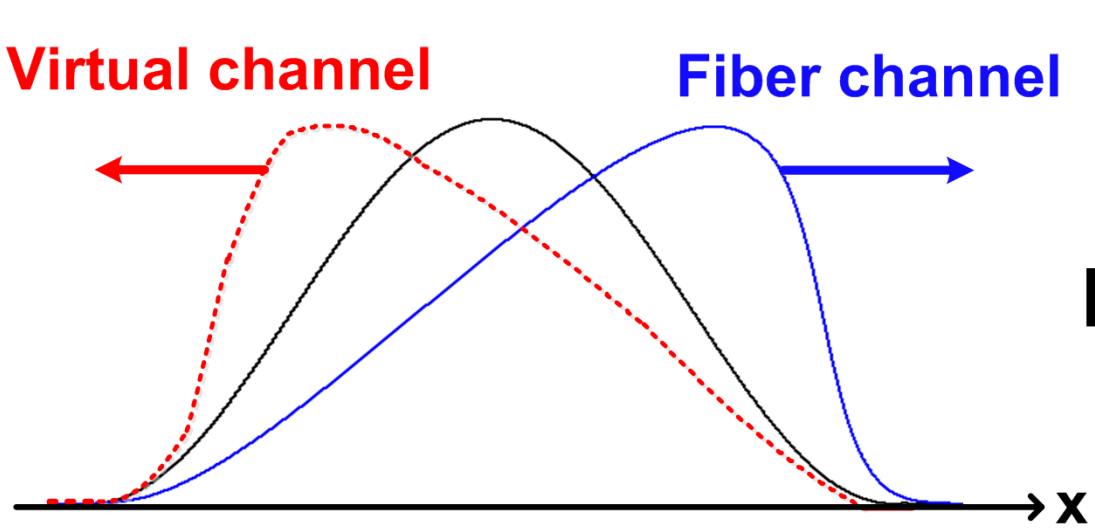
- **Virtual channel**



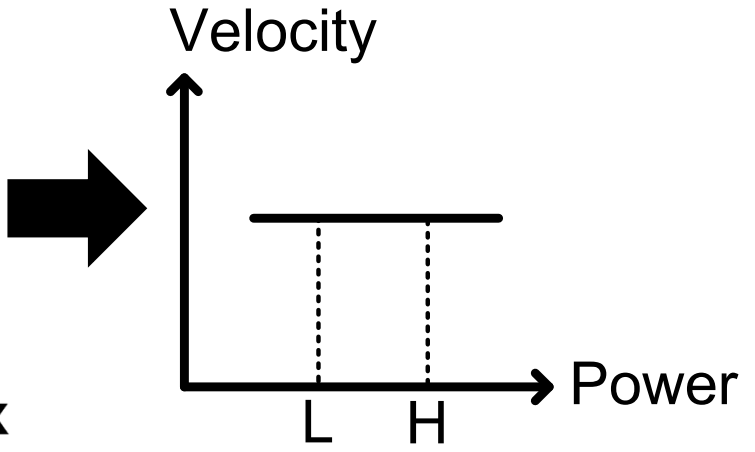


Nonlinear Filter Design for Tilting Compensation

- **Concept**



Optimized Channel



- **Modeling**

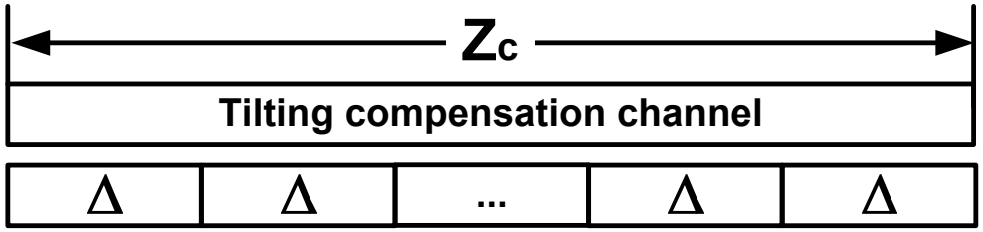
$$\frac{dP}{dt} + \beta(H + L - P)\frac{dP}{dx} = 0$$

Fiber dispersion, Laser chirp coefficient

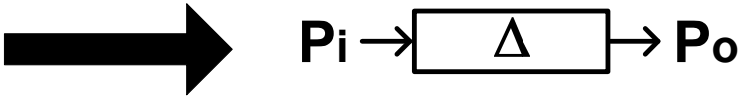
Nonlinear Filter for Tilting Compensation

Conversion into an implementable form

- **Spatial quantization**



$Z_c = \Delta \times N_{st}$



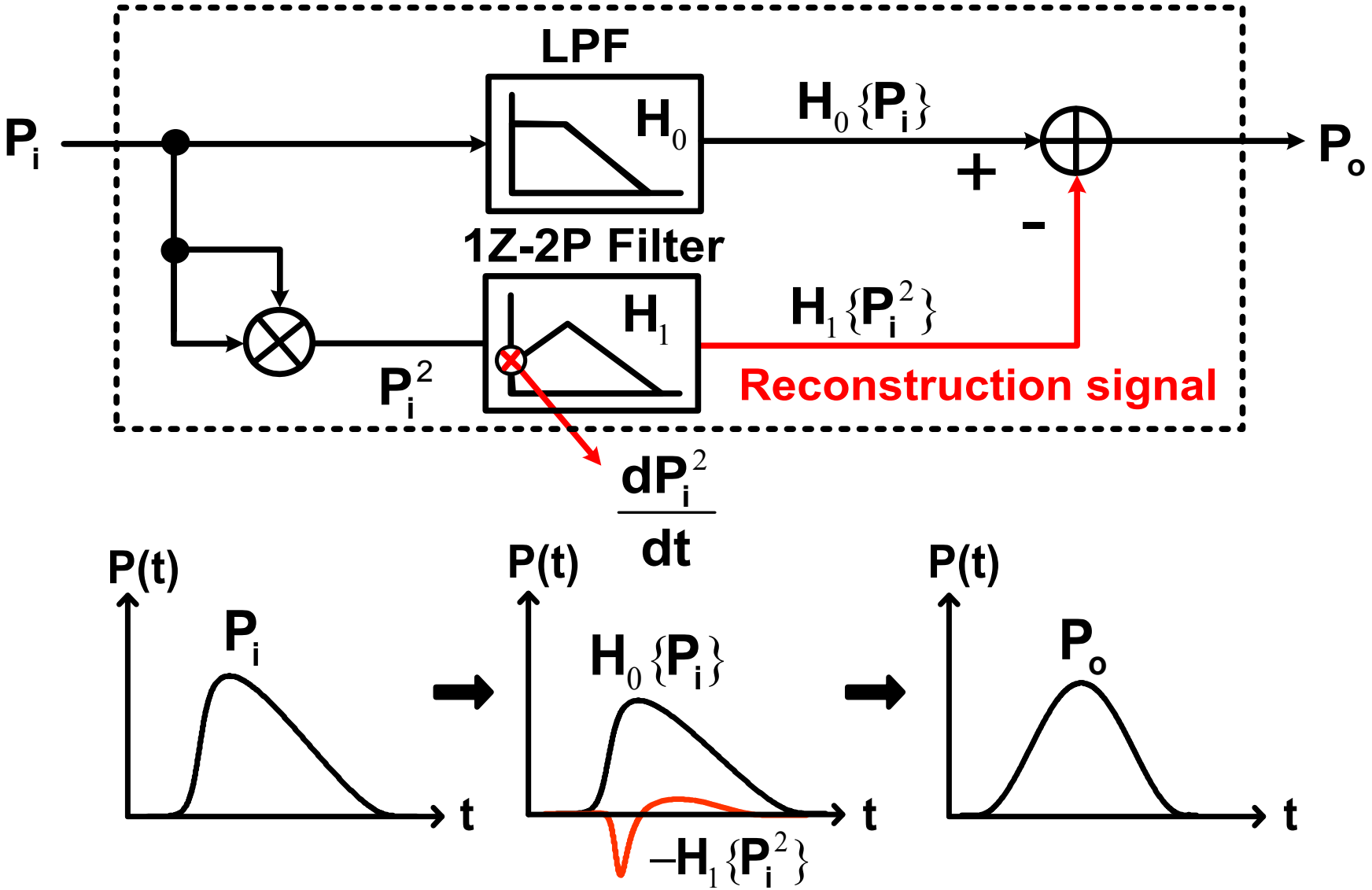
$$\frac{dP_o}{dt} + \beta(H + L - P_i)\frac{P_o - P_i}{\Delta} = 0$$ → **Nonlinear**

- **Volterra series expansion** $P_o(t) = H_o \circ P_i(t) - H_1 \circ P_i^2(t)$

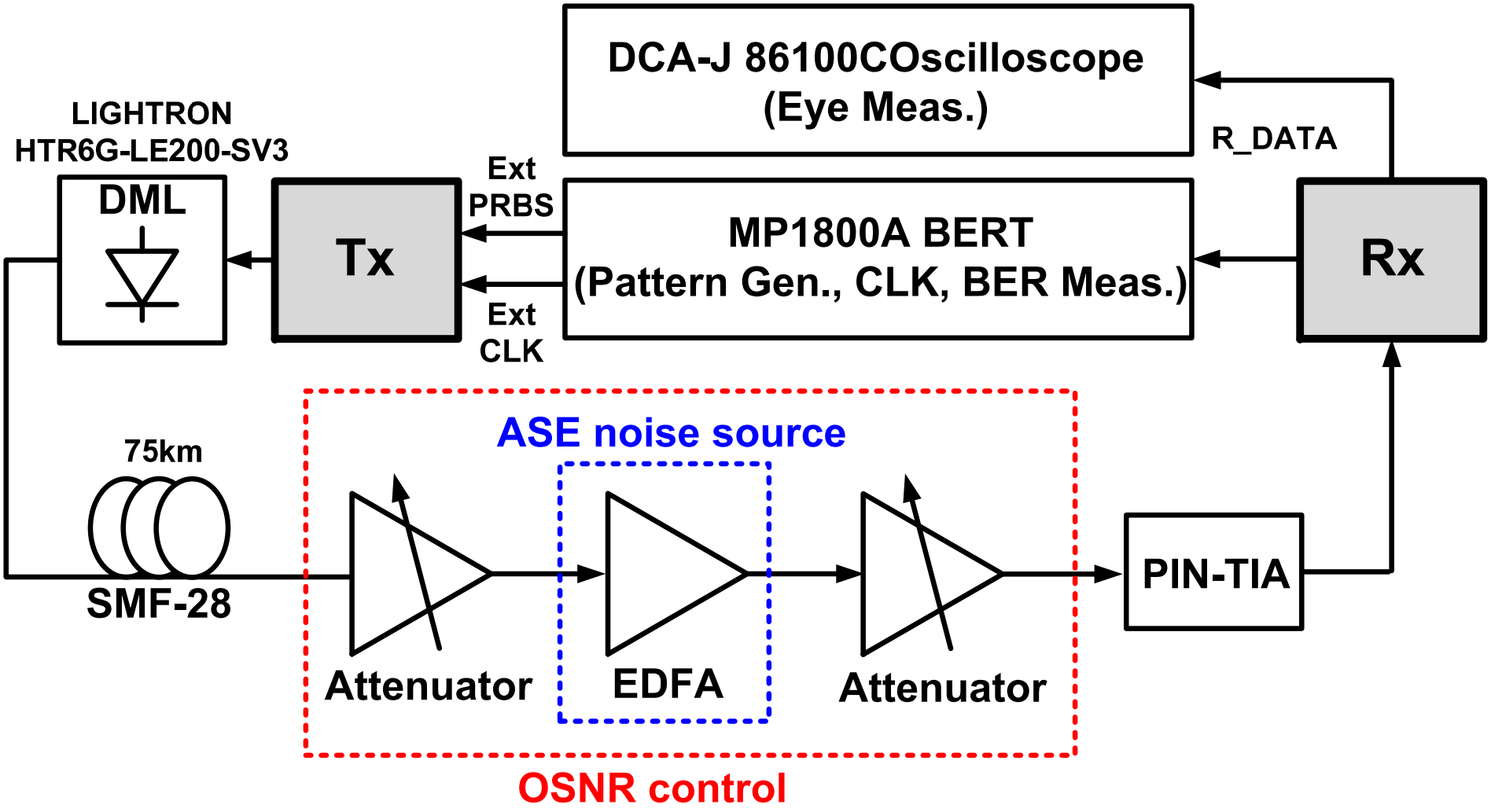
$$P_o(t) = \left[\frac{p_c}{s + p_c}\right] \circ P_i(t) - \frac{p_c}{H + L}\left[\frac{s}{(s + p_c)^2}\right] \circ P_i^2(t)$$

H_0 **H_1** → **Simple zero-pole filter**

Tilting Compensator Implementation

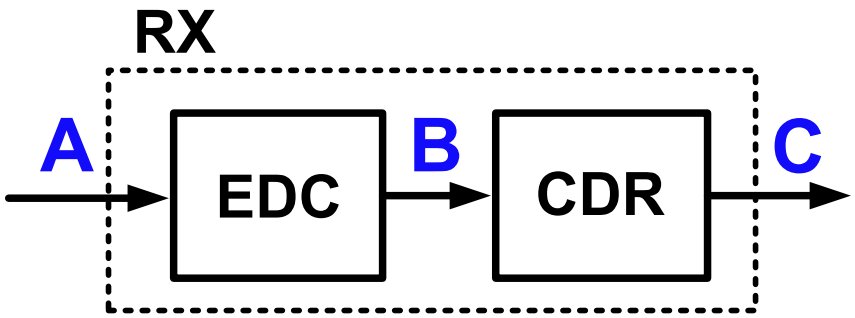


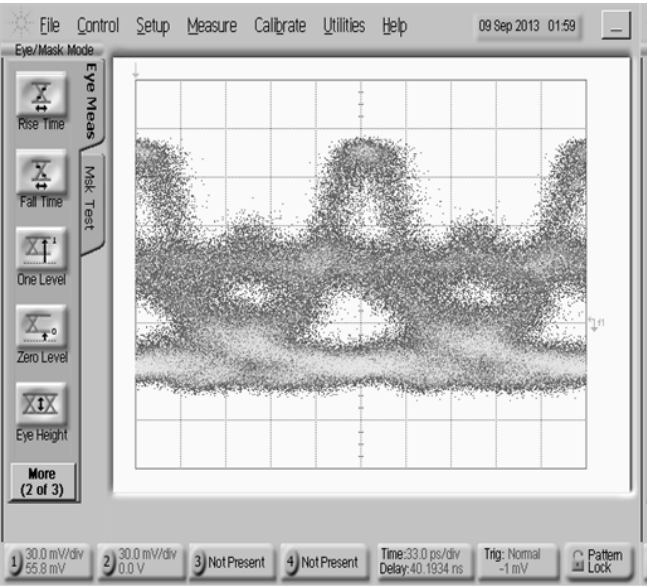
Experimental Setup

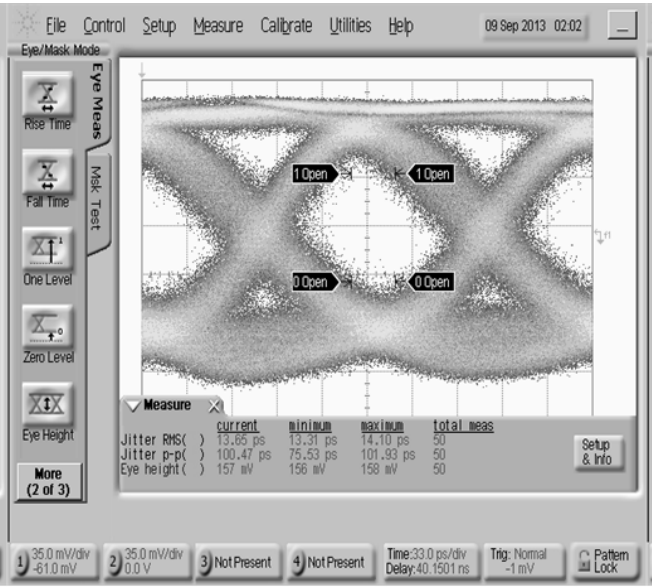


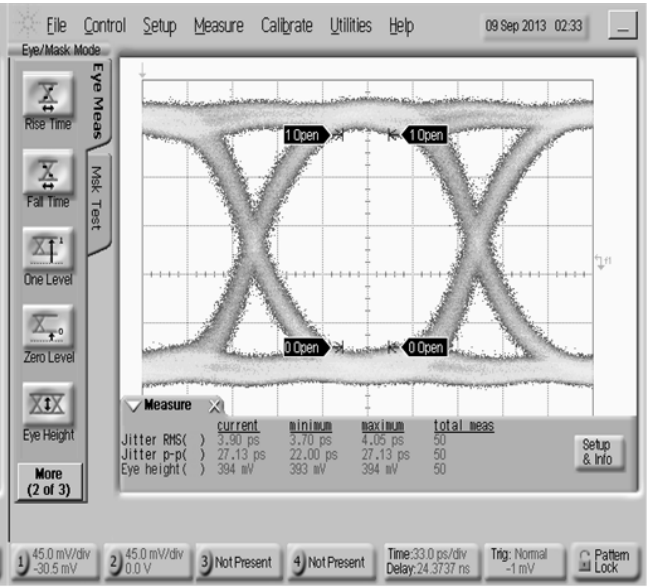
Eye Measurement

- 75km transmission
- 6Gb/s NRZ sequence







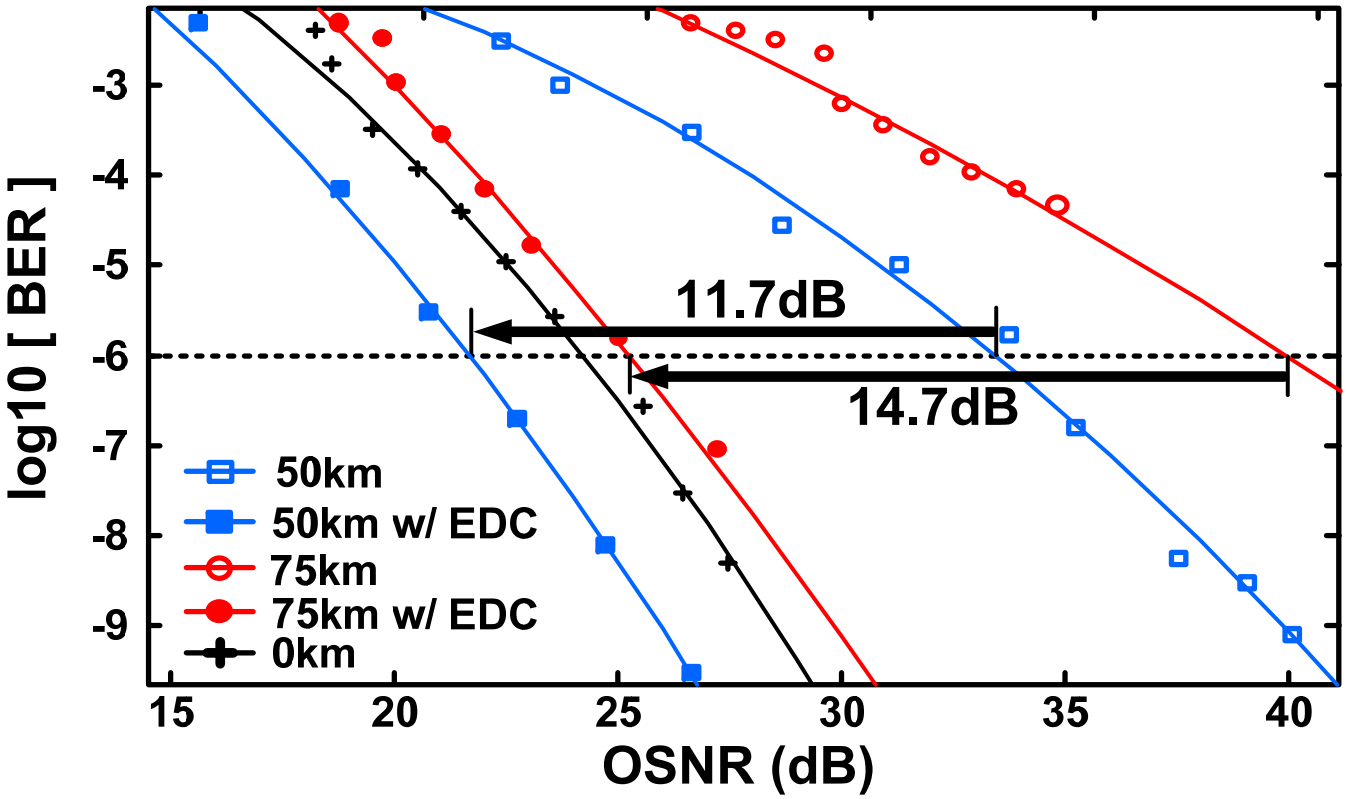


A. Before EDC **B. After EDC** **C. After CDR**

BER Measurement

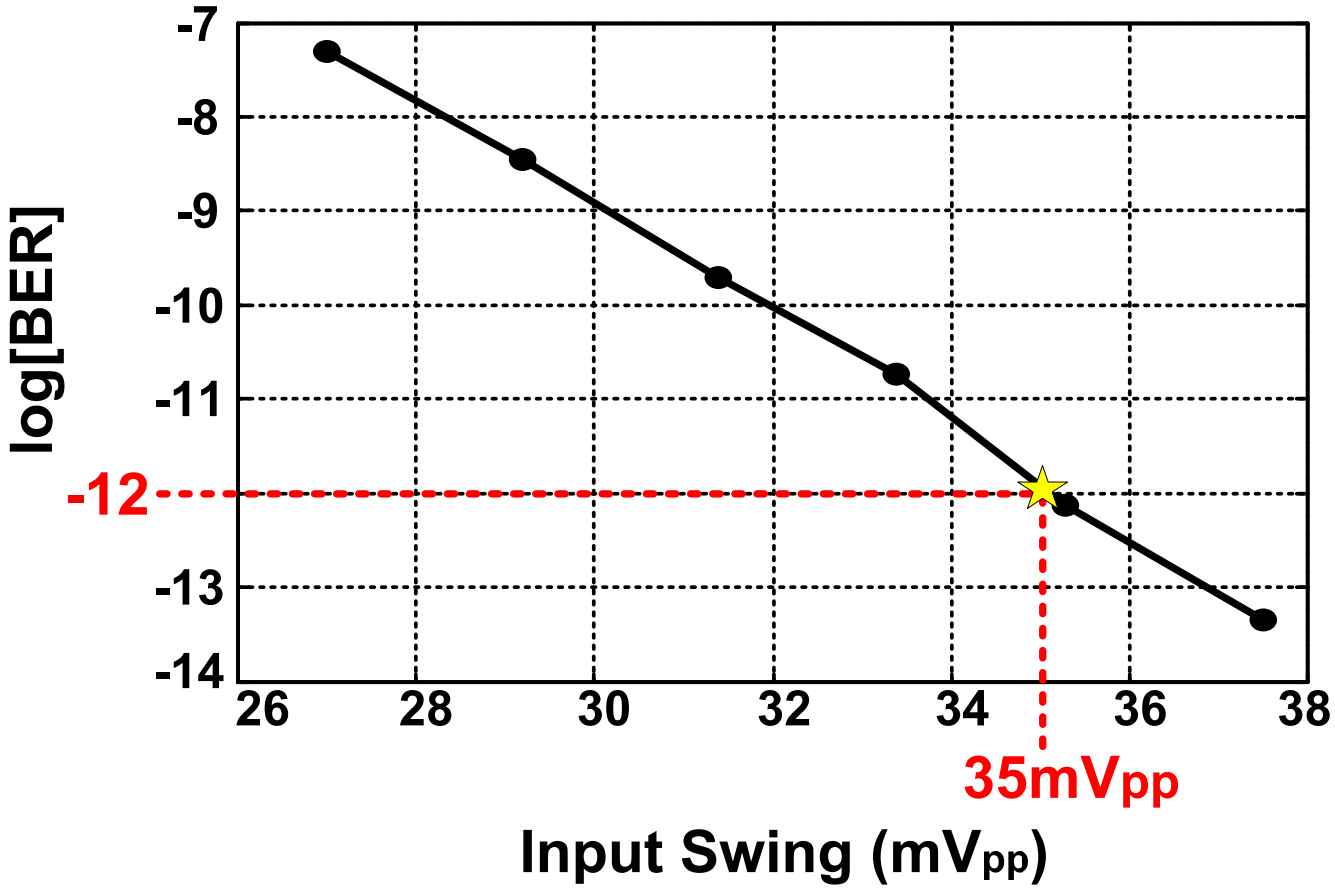
OSNR improvement

- At a BER of 10^{-6} , 11.7dB at 50km and 14.7dB at 75km

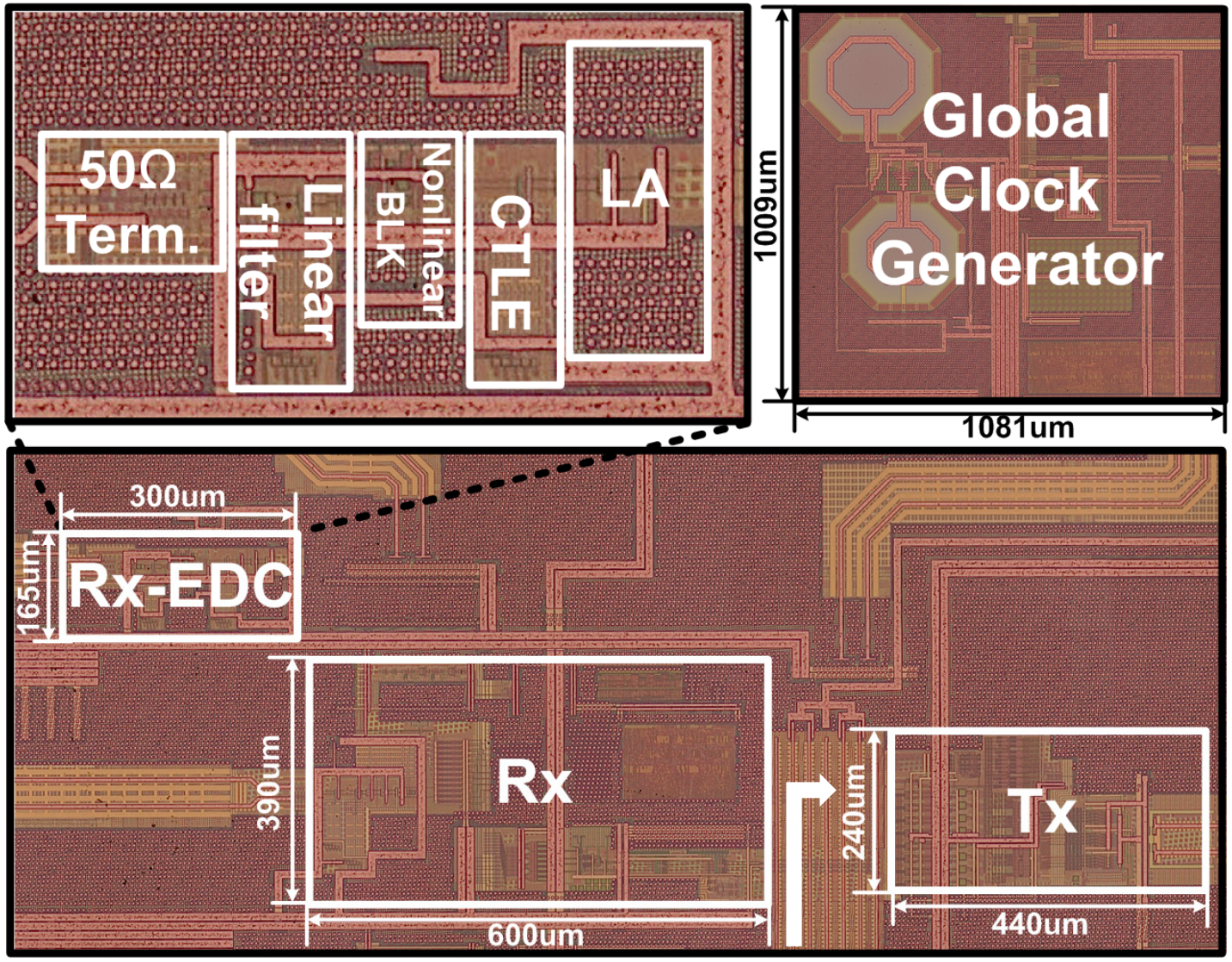


Input Sensitivity

- At a BER of 10^{-12} , 35 mV_{pp}



Chip Microphotograph



System Summary

Technology		90nm CMOS
Supply voltage		1 V
Data Rate		6Gb/s
Active Area	Tx	0.106 mm²
	Rx	0.240 mm²
	Rx-EDC	0.050 mm²
	Global clock generator	1.091 mm²
Total Active Area		1.487 mm²
Power Consumption	Tx	45.6 mW
	Rx	56 mW
	Rx-EDC	22.4 mW
	Global clock generator	102 mW
Total Power		226mW

Conclusions

- The first nonlinear EDC to overcome chirp-induced dispersion of a low-cost DML
- 15dB OSNR improvement at the BER $\text{of } 10^{-6}$ in 75km SMF-28
- Extend the reach of DML in upstream FTTH and LTE backhaul
- Replace EML in downstream FTTH and metro access network

Paper 8.2:
A 12×5 Two-Dimensional Optical I/O Array for 600Gb/s Chip-to-Chip Interconnect in 65nm CMOS

Hiroshi Morita, Koki Uchino, Eiji Otani, Hiizu Ohtorii,
Takeshi Ogura, Kazunao Oniki, Shuichi Oka,
Shusaku Yanagawa, Hideyuki Suzuki

Sony Corporation, Tokyo, Japan

Outline

- Motivation
- Architecture
- Circuit Design
- Measurement Results
- Summary

Motivation

Chip-to-chip or board-to-board wide-bandwidth interconnects in high-performance systems such as supercomputers or high-end servers

Requirement

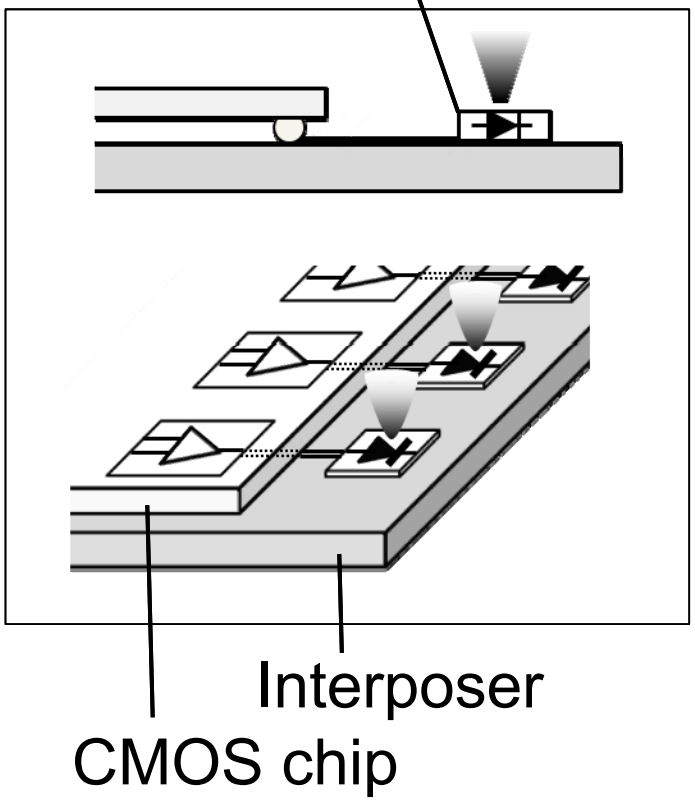
- Terabit-per-second total bandwidth

Our approach

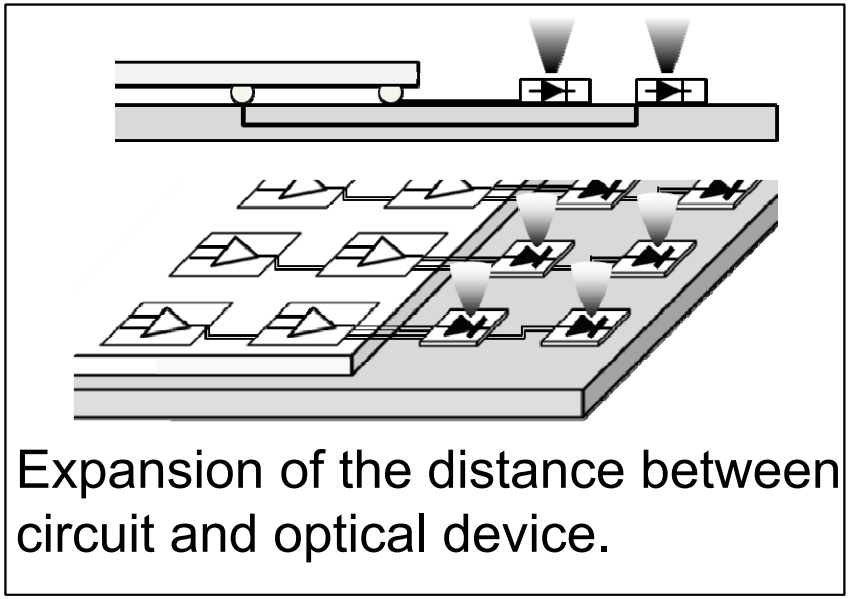
- Multi-channelization

Implementation Approach

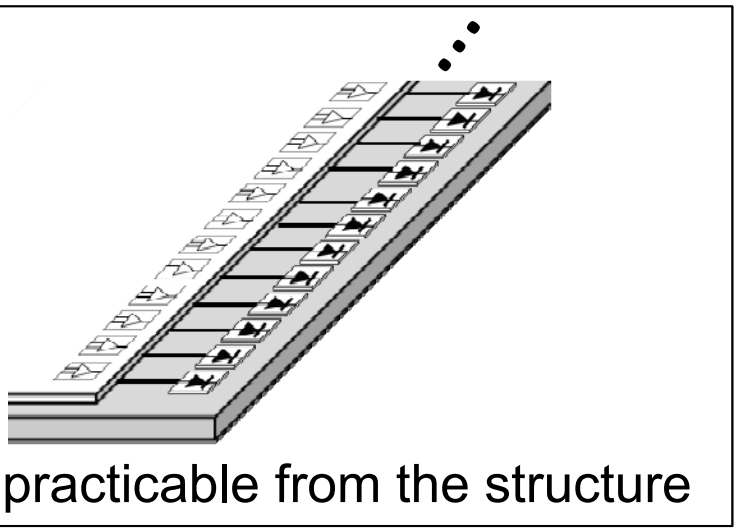
Conventional architecture



Multi Channel



Expansion of the distance between circuit and optical device.

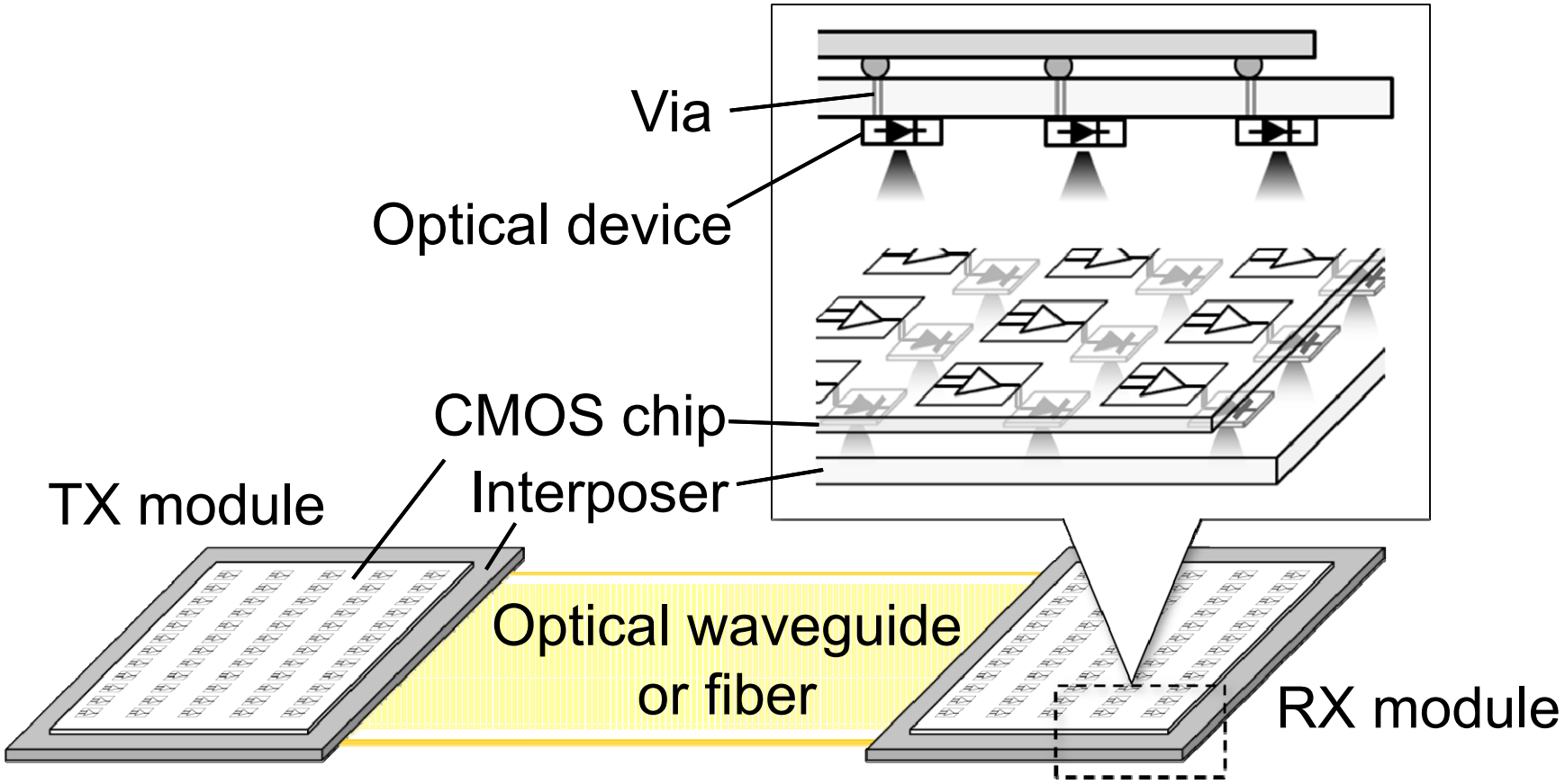


No practicable from the structure

Implementation Approach

Two-dimensional optical I/O array

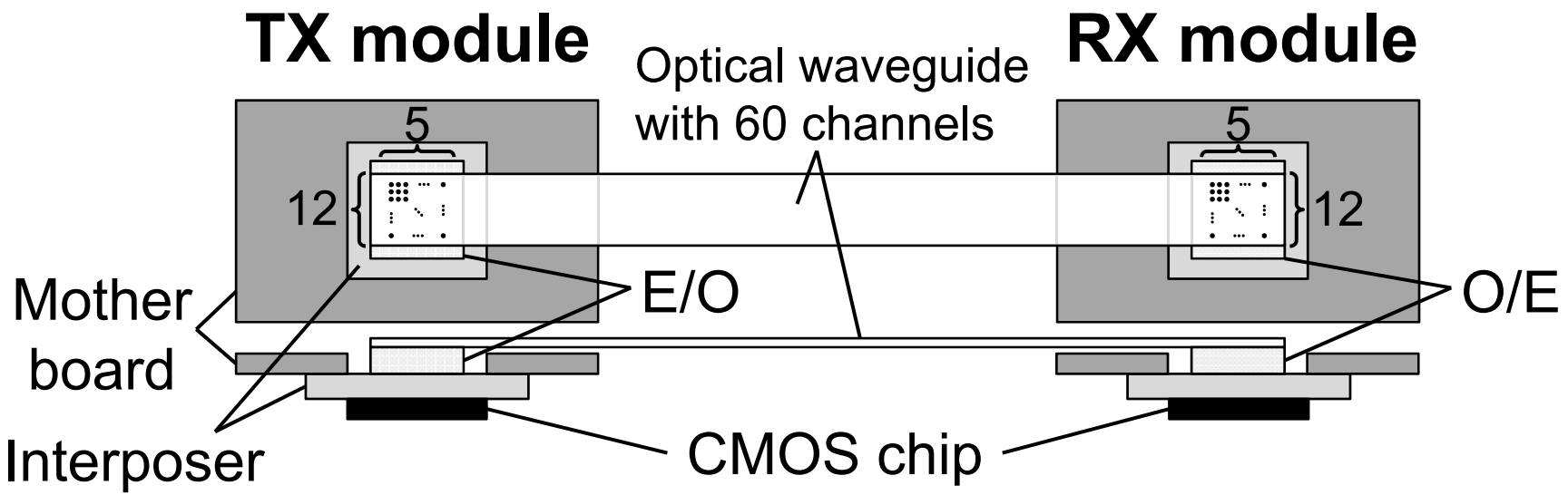
- Less parasitic by via of short distance
- No physical limitation for number of channels



Outline

- Motivation
- Architecture
- Circuit Design
- Measurement Results
- Summary

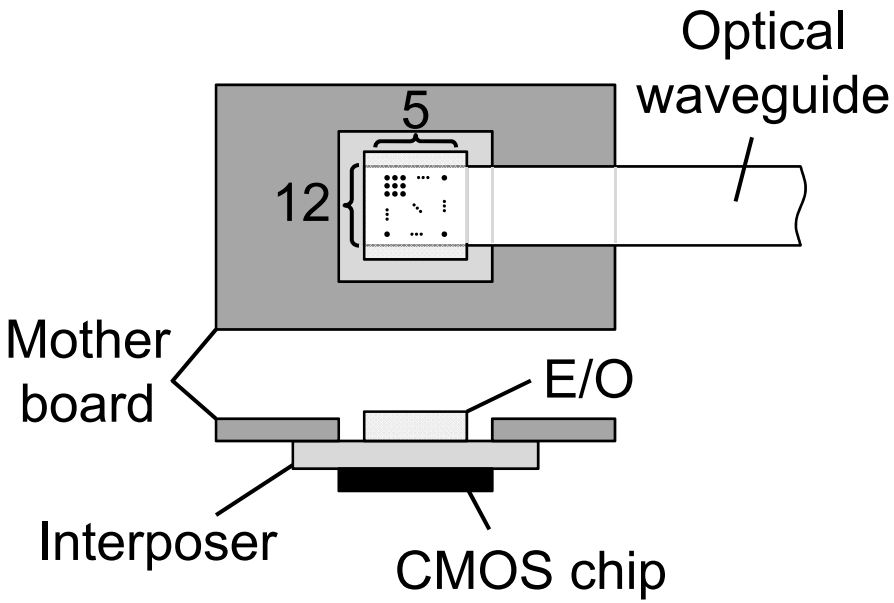
Transmission System Diagram

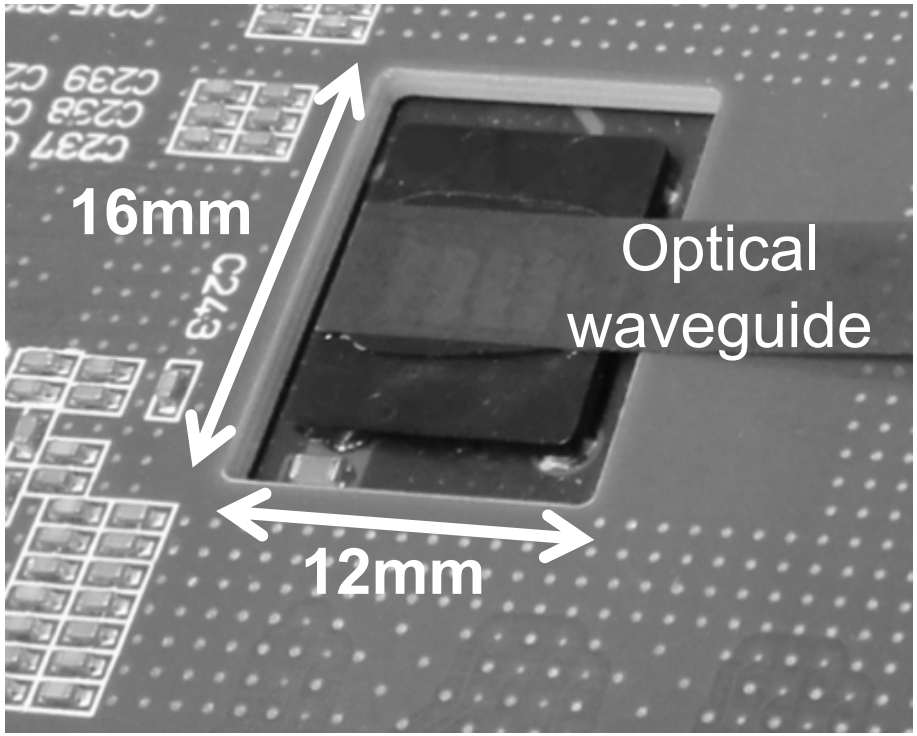


# of Channels	Speed/ch [Gb/s]	Total bandwidth [Gb/s]
12 × 5 = 60	**10**	**600**

Trial Module

Chip-to-chip or board-to-board communications with compact and thin connector





Outline

- Motivation
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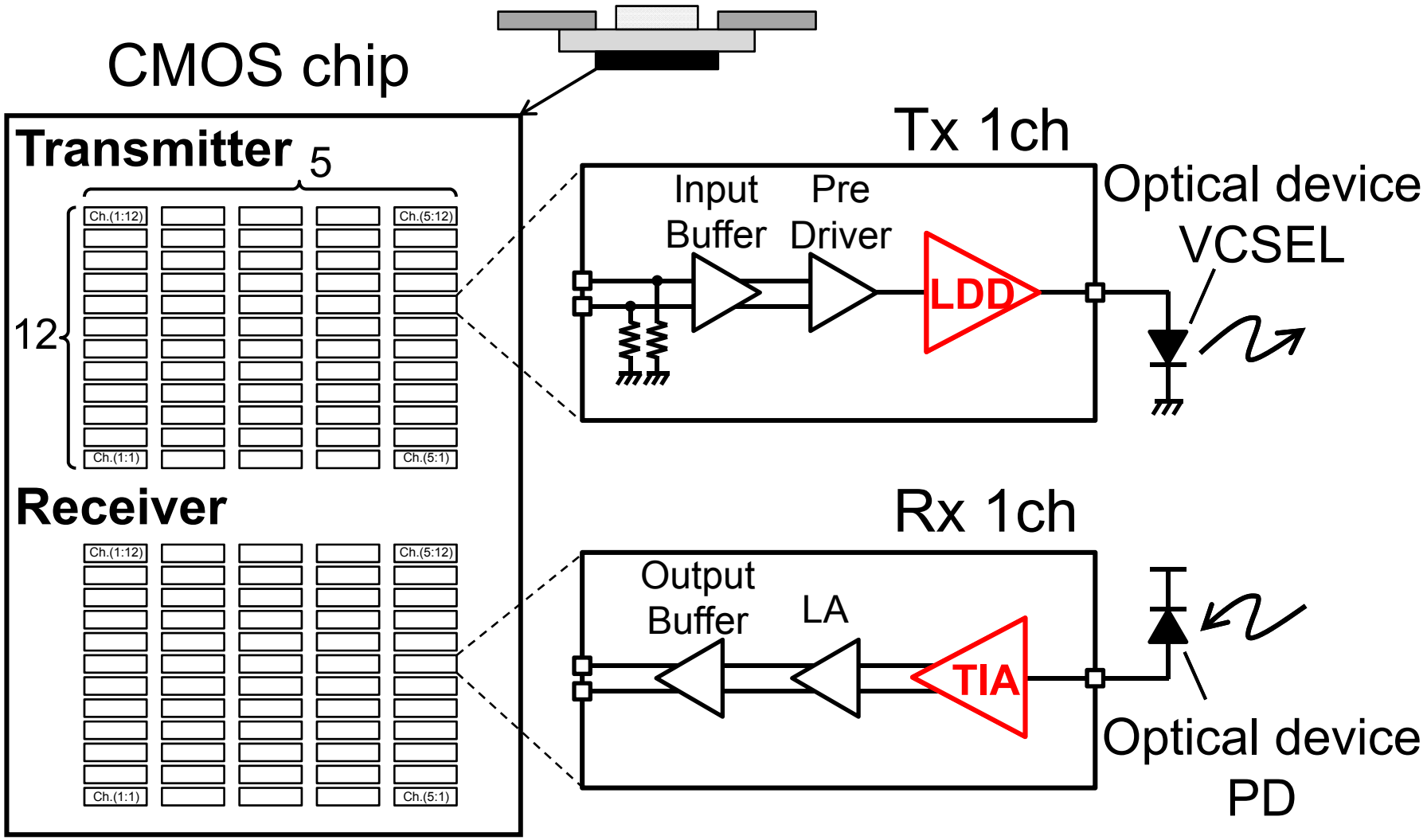
- Summary

CMOS Chip Block Diagram



Requirements

The LDD in the transmitter

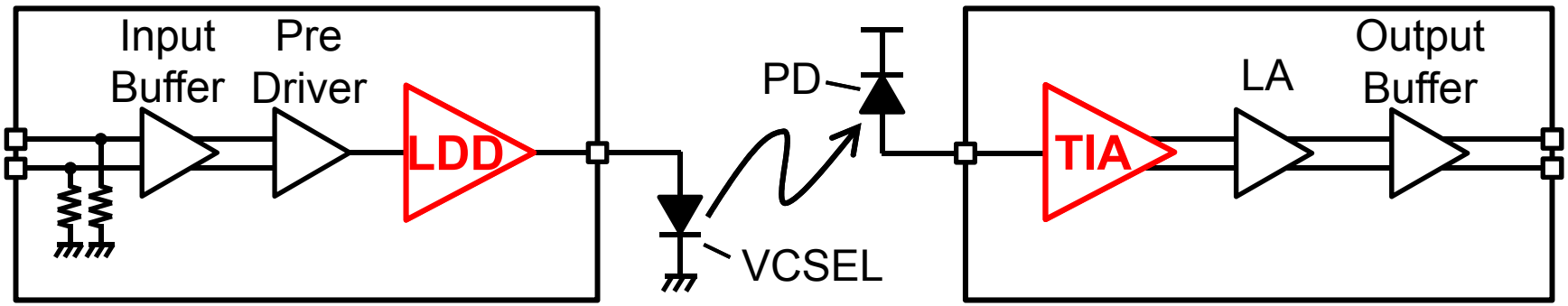
- Low power consumption

  Cooling system for VCSEL can be simplified

The TIA in the receiver

- Low noise

  Power budget for the optical communication system can be eased



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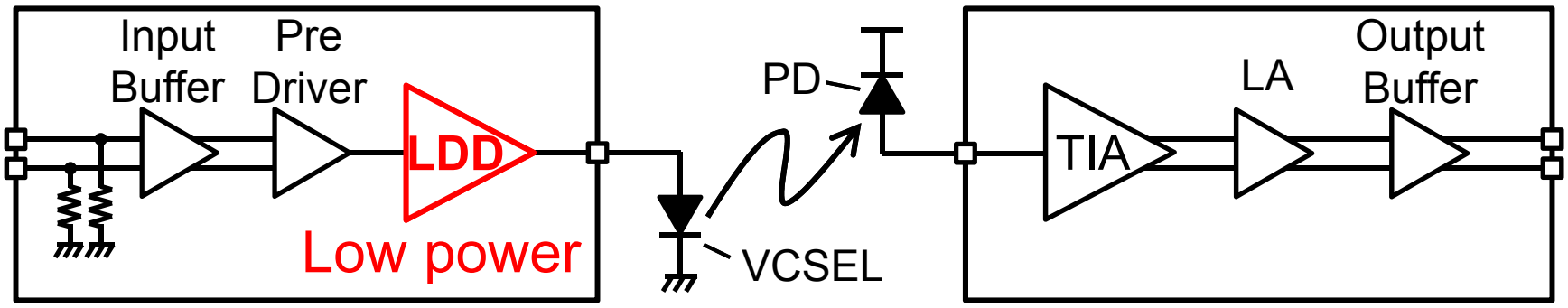
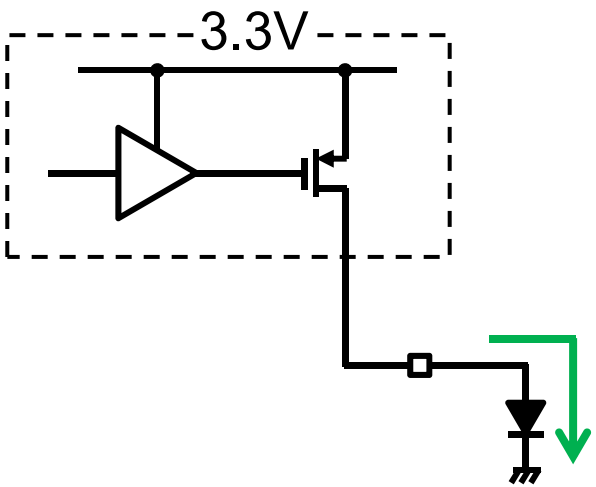
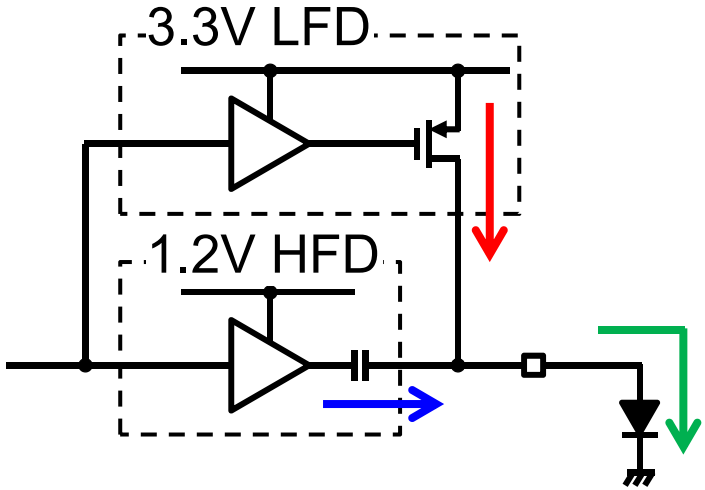
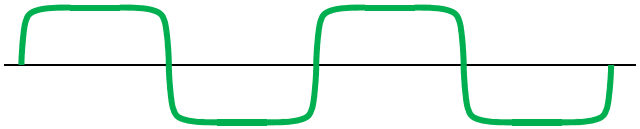
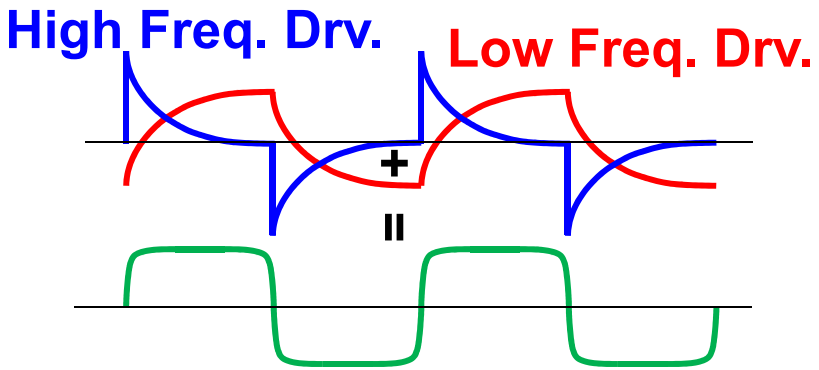
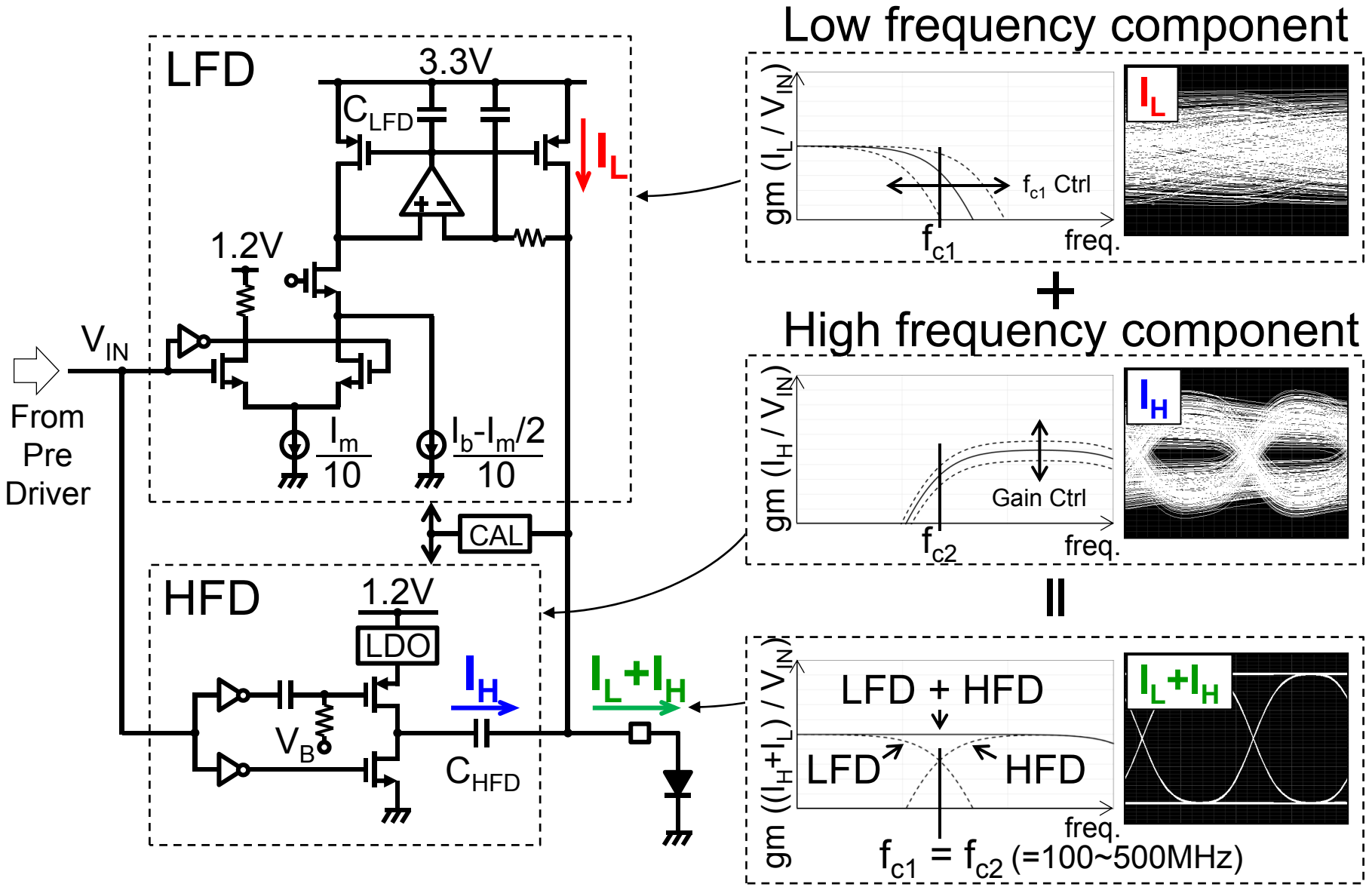


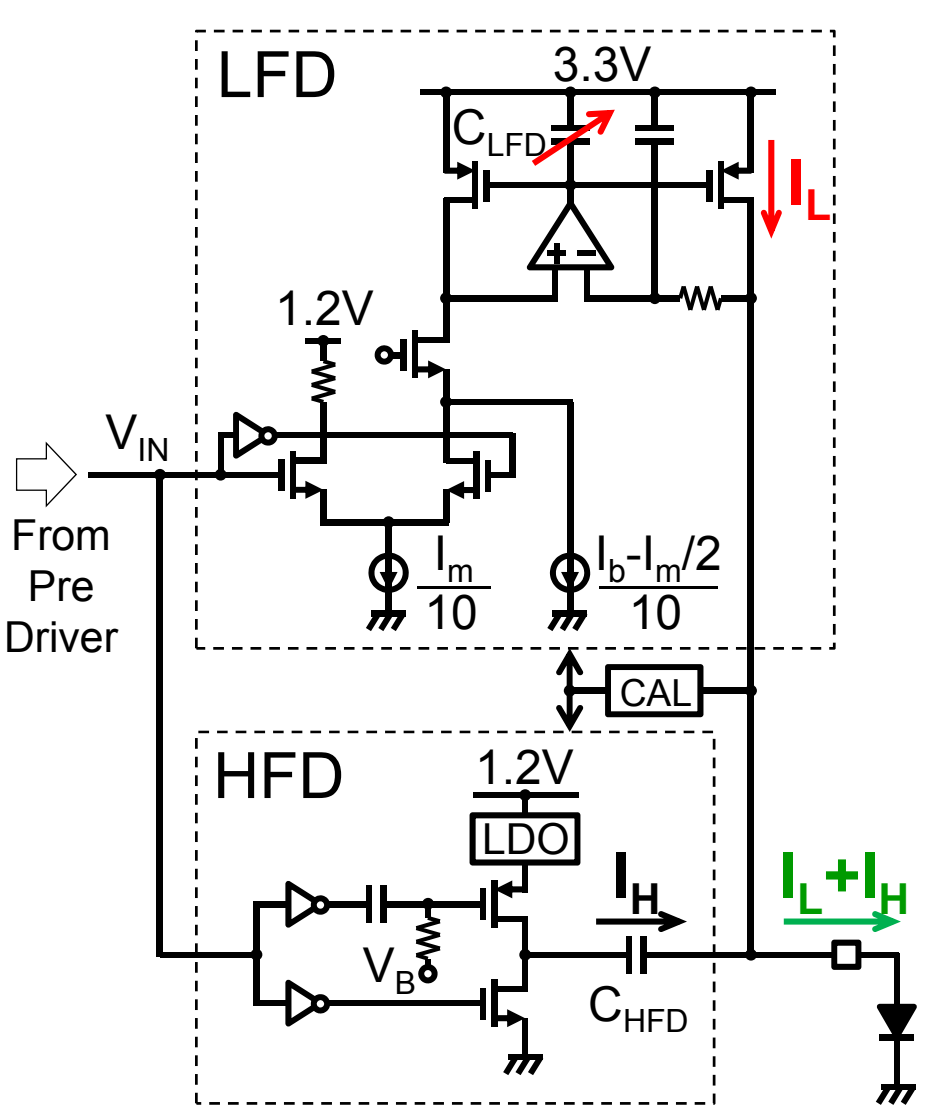
LDD Topology

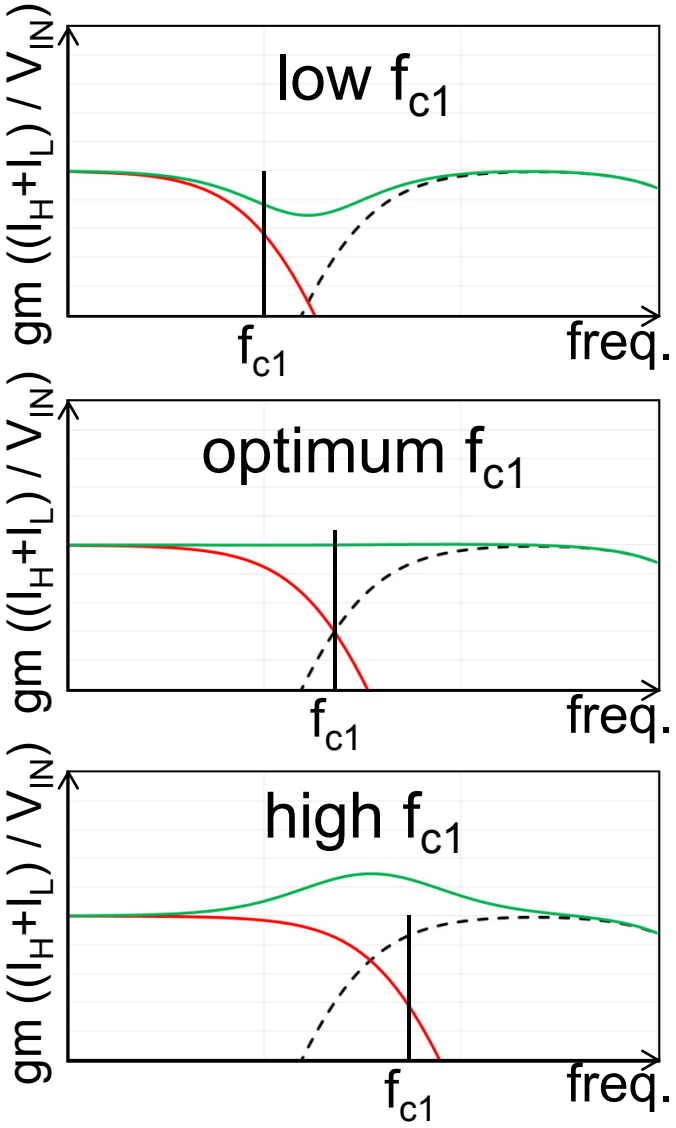
	Conventional	HFD + LFD
Block Diagram		
Concept		
Power	**High**	**Low (40% down)**

LDD Circuit

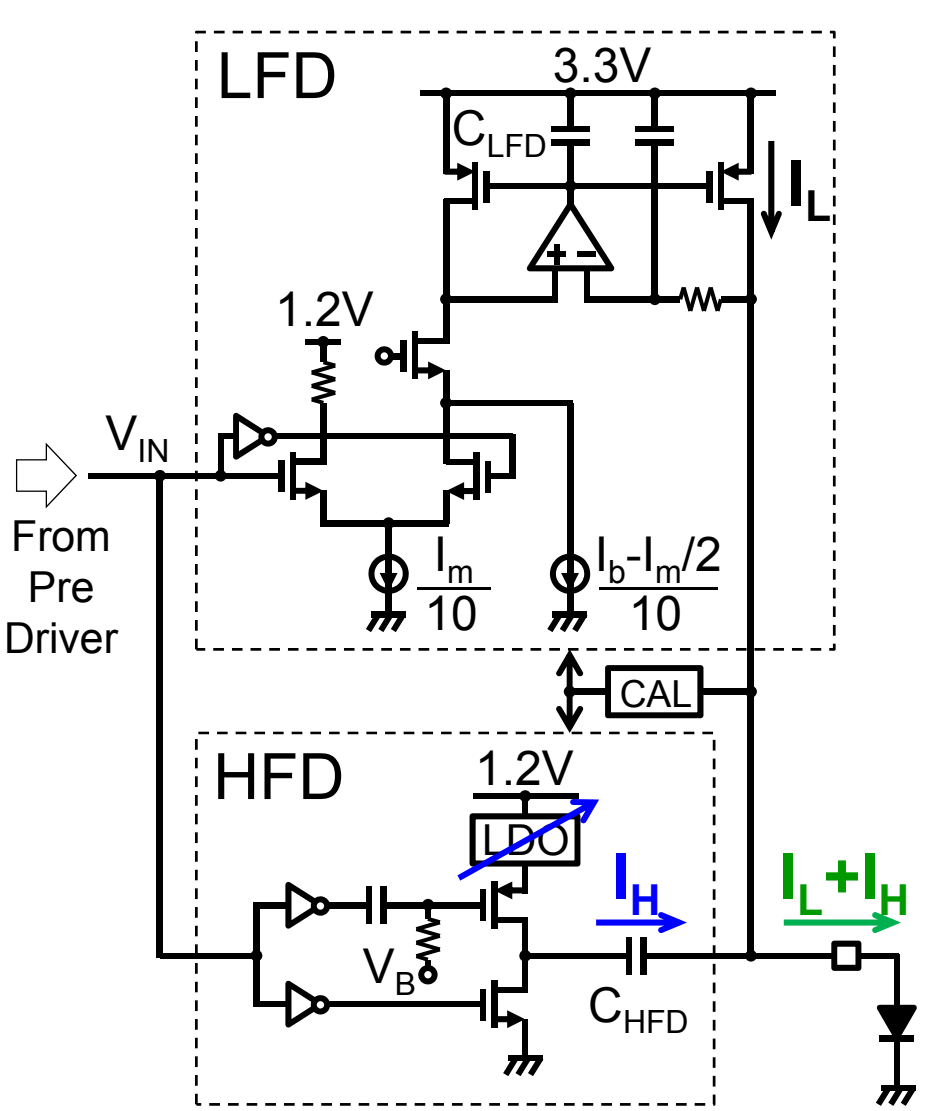


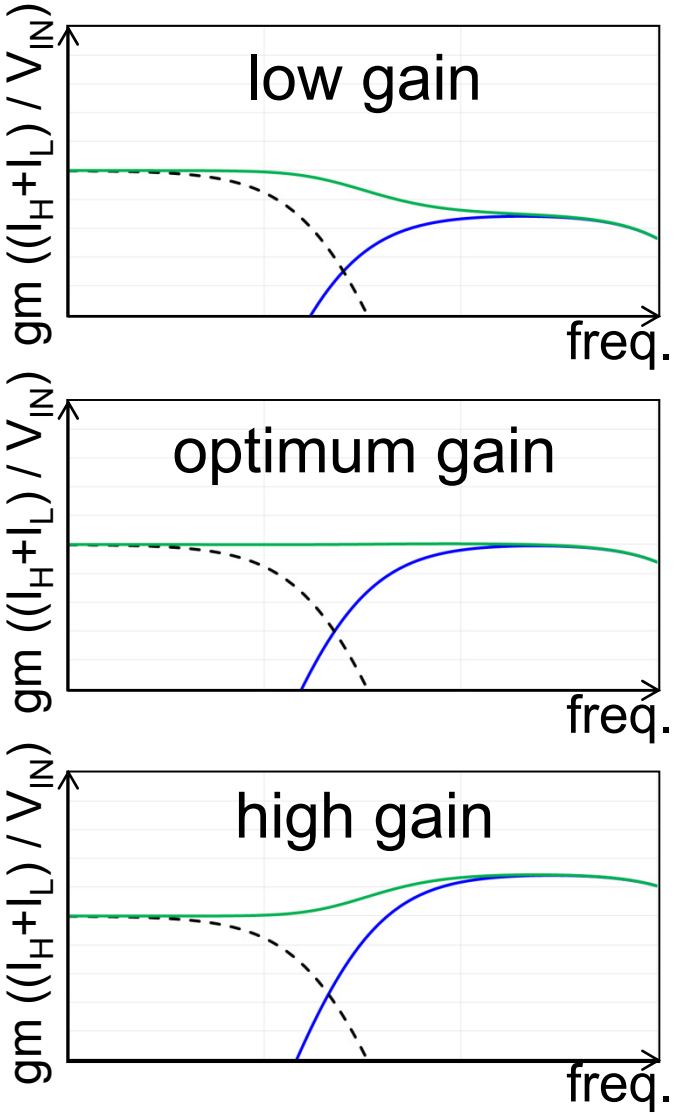
Calibration of LFD





Calibration of HFD





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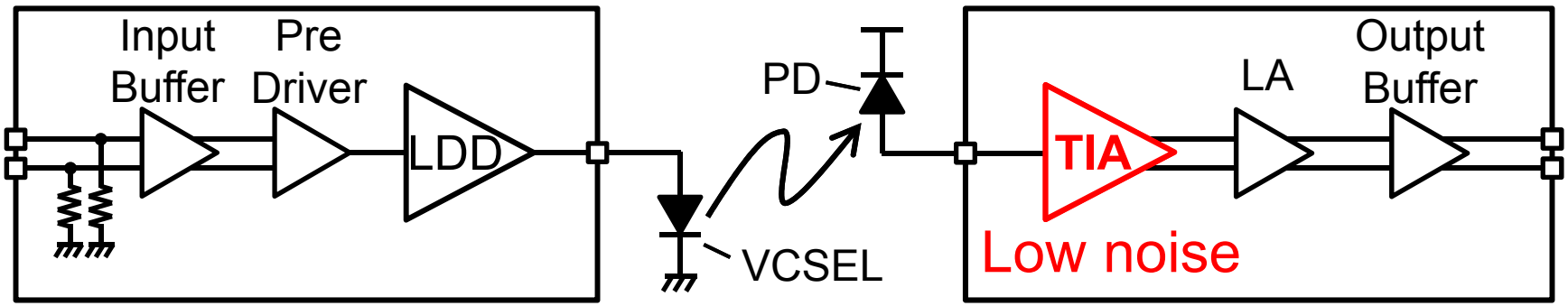
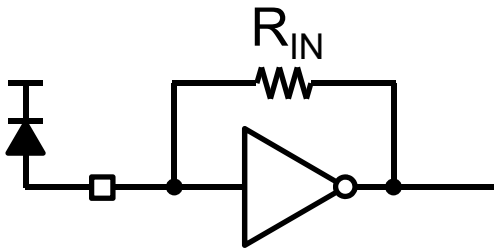
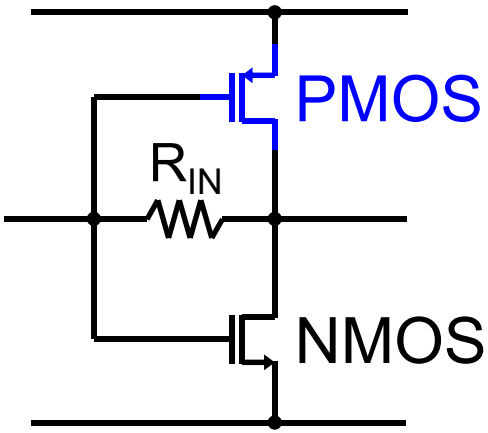


Features of CMOS Inverter

Advantage : low noise





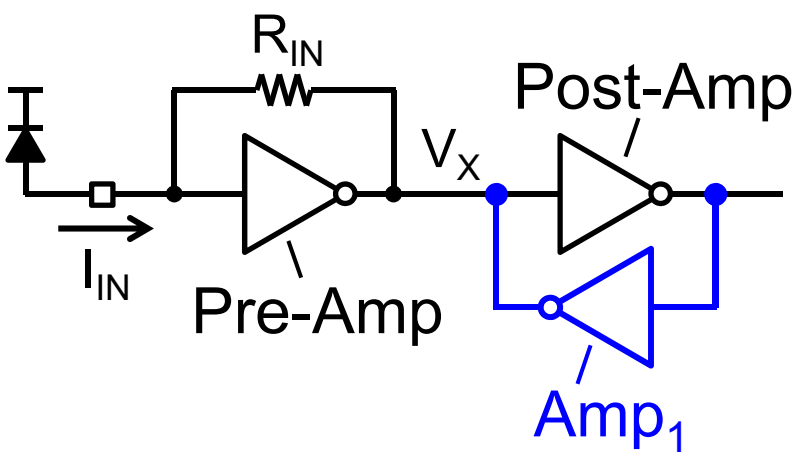
Thermal noise of MOSFET

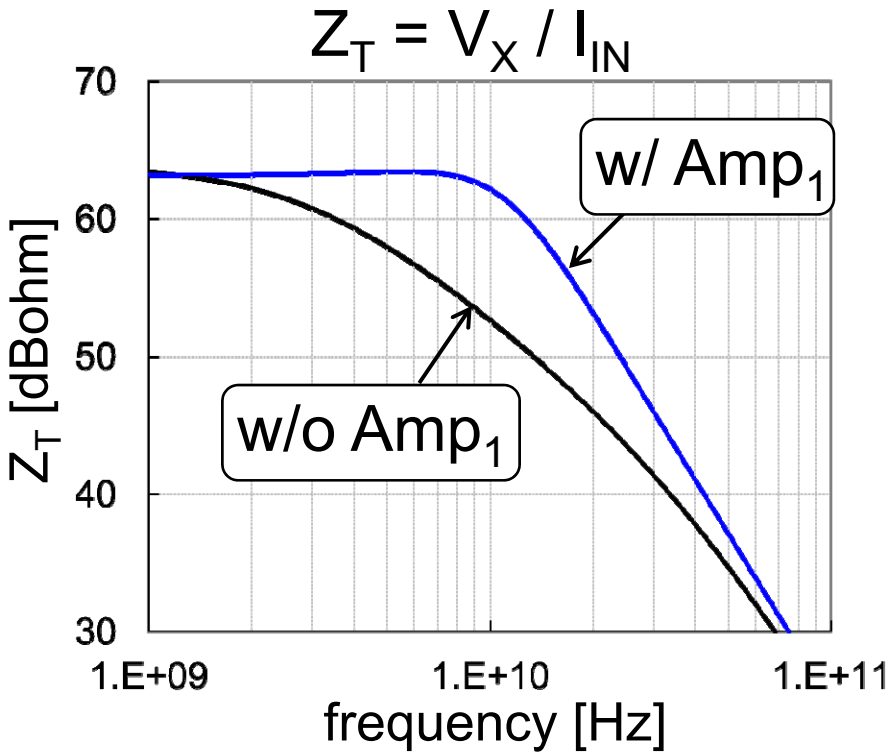
$$I_{noise} = \sqrt{4KT\gamma g_m}$$

$$\gamma_{NMOS} \approx 4 \times \gamma_{PMOS}$$

Disadvantage : low bandwidth

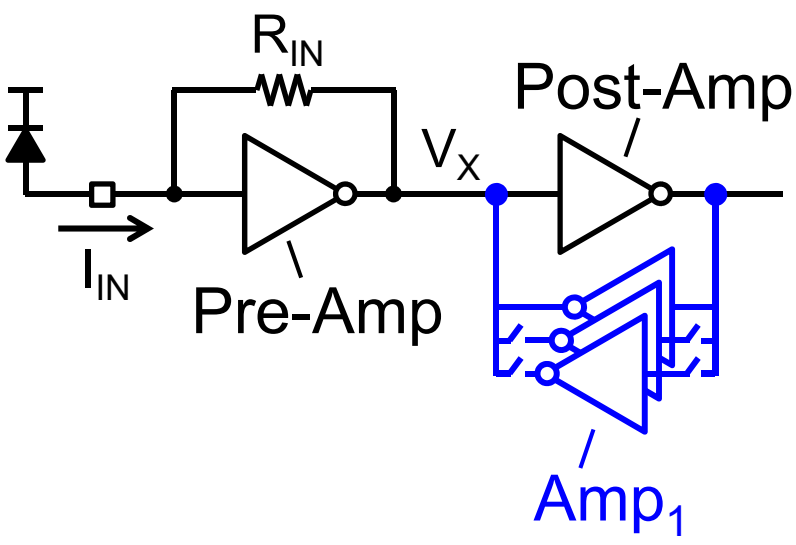
Bandwidth Enhancement

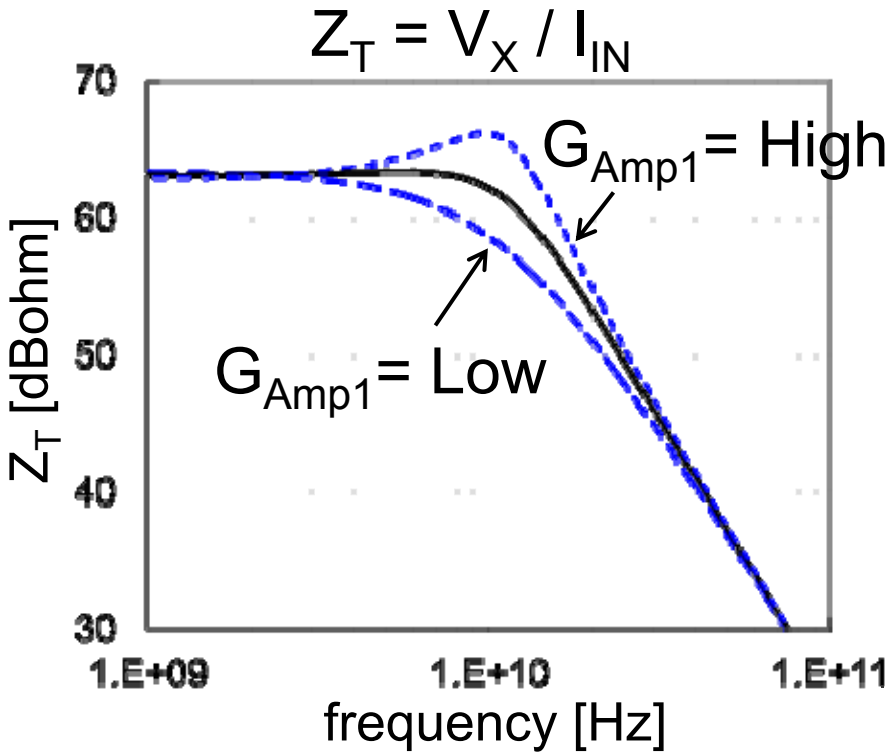




- In order to further reduce input-referred noise, large size of pre-amp and RIN is required
- Adding Amp1 compensates bandwidth degradation

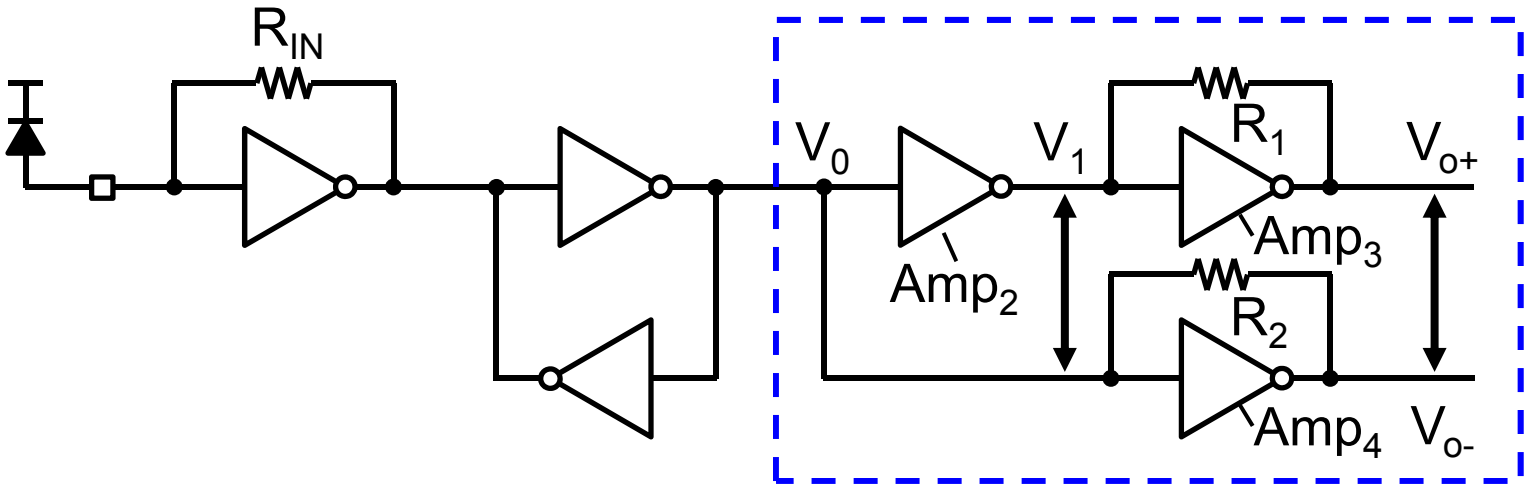
Compensation for the BW degradation





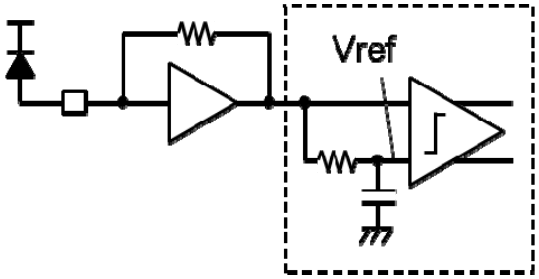
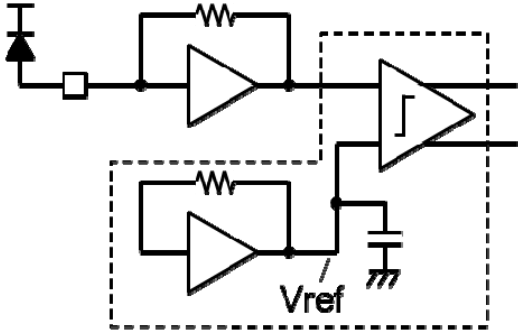
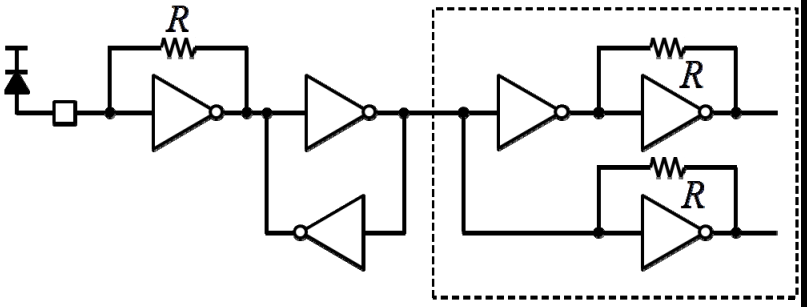
- Bandwidth is adjusted by Amp_1 gain
- Amp_1 is automatically set to the optimum value during the initialization process to absorb process variation

Single-end-to-Differential Converter

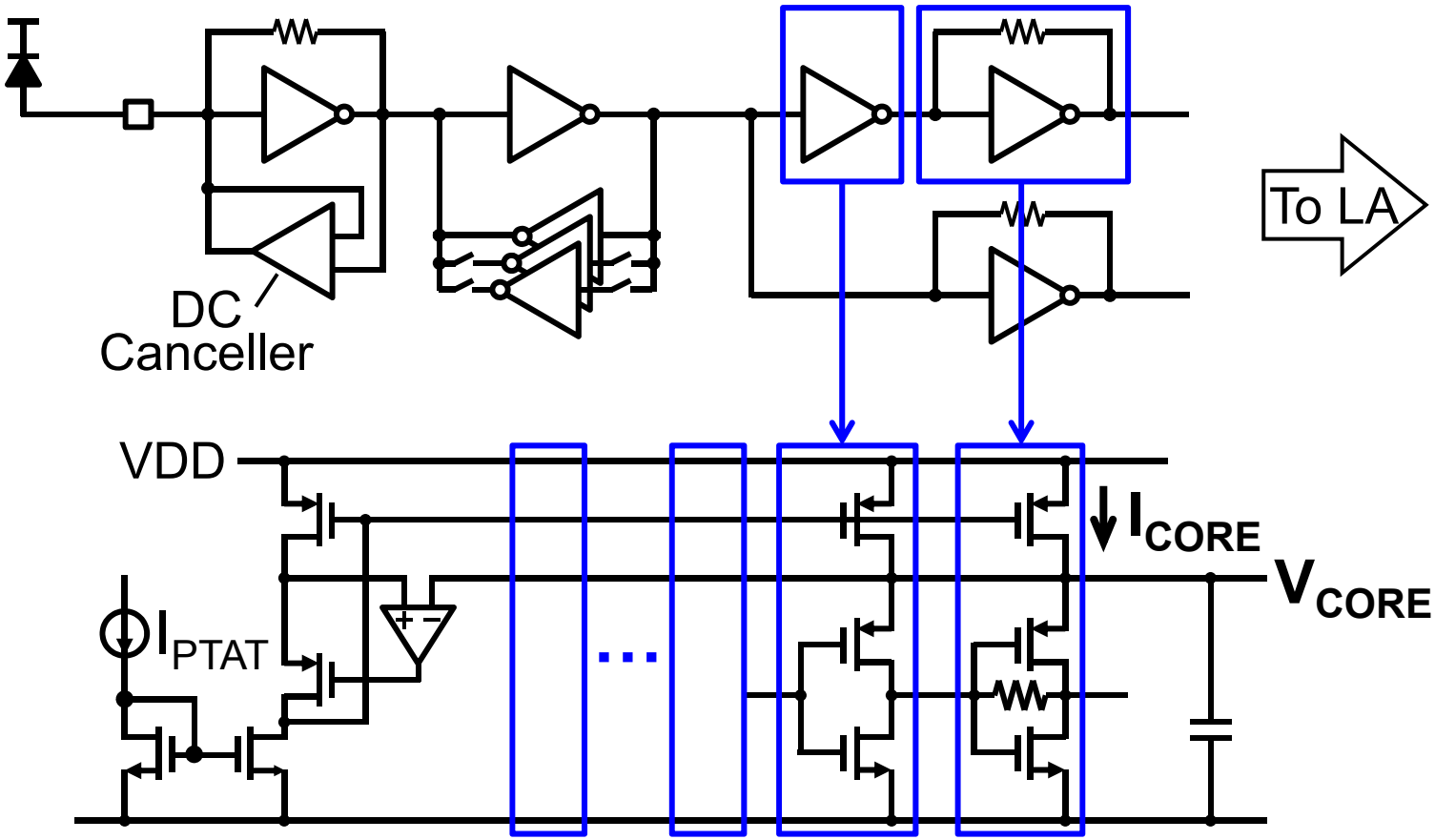


- Amp_2 together with the two self-biased amplifiers enable single-ended to differential conversion without a reference voltage
- Amp_2 gain is controlled to -1 by the combination of R_1 and Amp_3

Comparison of S/D Converter Topologies

Type	Architecture	Size	Power
Conventional RC Filter		Large	Low
Conventional Replica		Large	High
This work Self Biased		**Small**	**Low**

TIA Block Diagram



- All of the amplifiers are composed of CMOS inverters
- PMOS current source absorbs PVT variation and maintains constant BW

Outline

- Motivation
- Architecture
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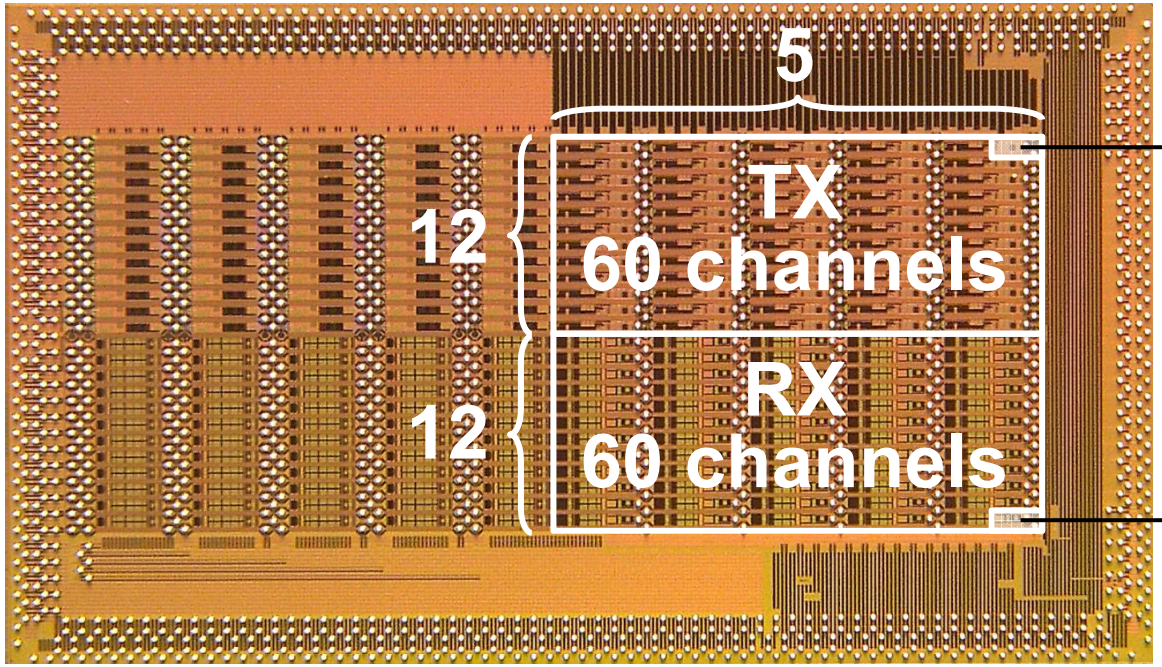
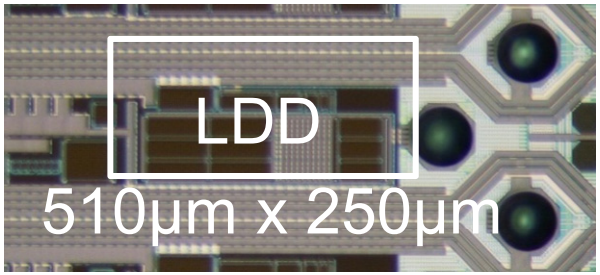
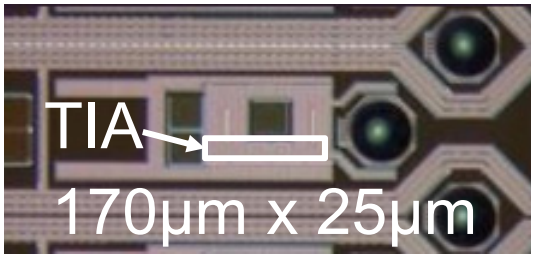
- Measurement Results
- Summary

Die Photo

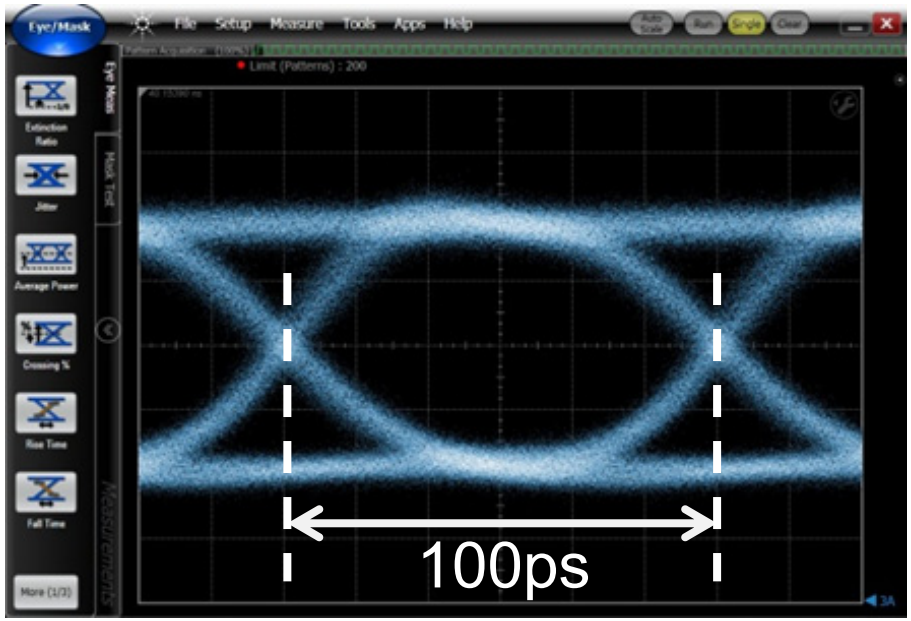






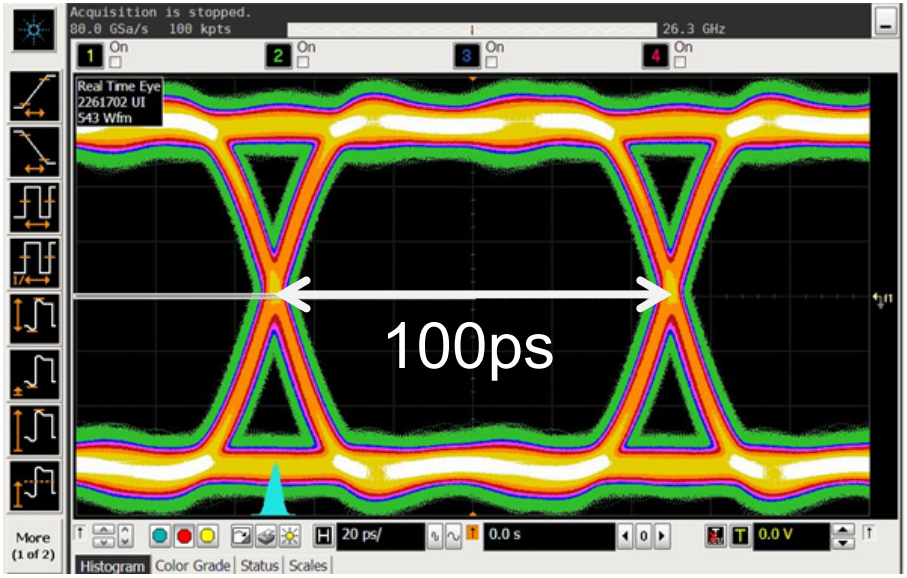
- Standard 65nm CMOS process
- Chip size : 18 × 10mm^2
- Pitch of LDDs and TIAs :
  - 250μm in the vertical direction
  - 1500μm in the horizontal direction

Transmitter Optical Eye



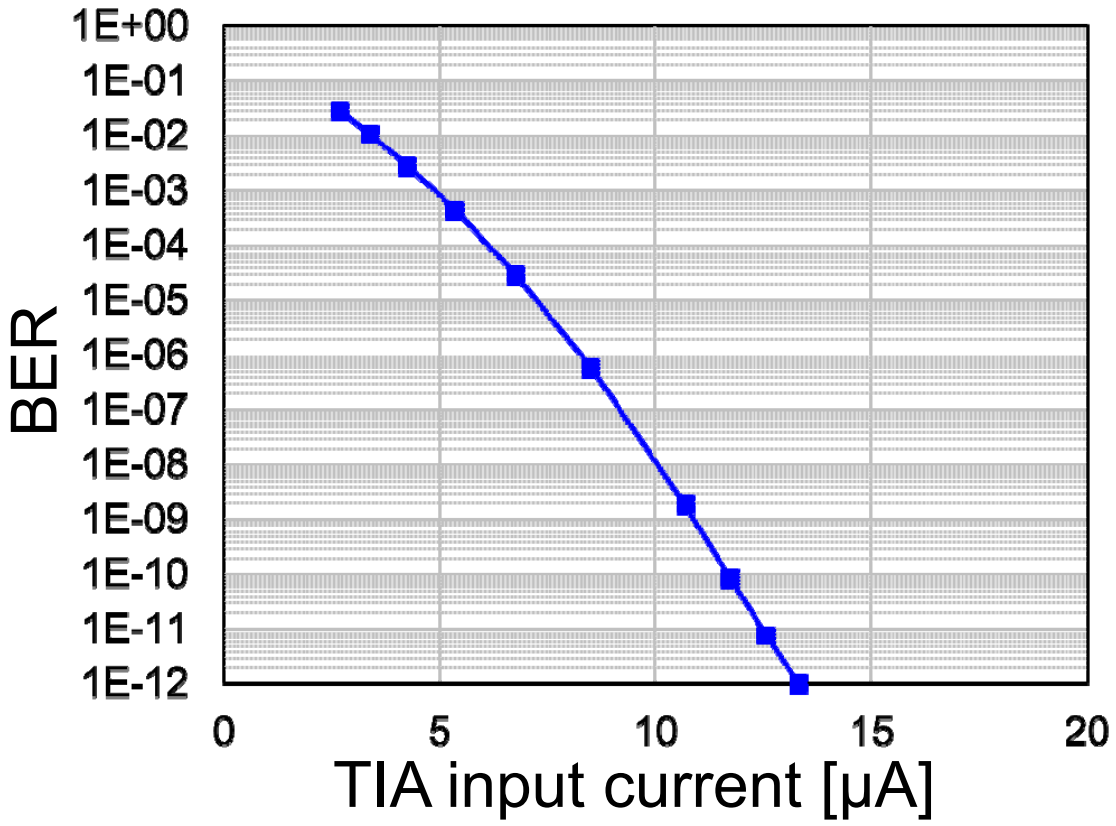
- 10Gb/s 2^7-1 PRBS
- One channel enabled
- Jitter : $22.4ps_{PP}$
- Pave = 5.9dBm, Poma = 6.4dBm
  (setting : Ibias = 7mA, Imod = 8mA)
- 21.7mW/ch (LDD block, w/o VCSEL @2V)

Receiver Electrical Eye



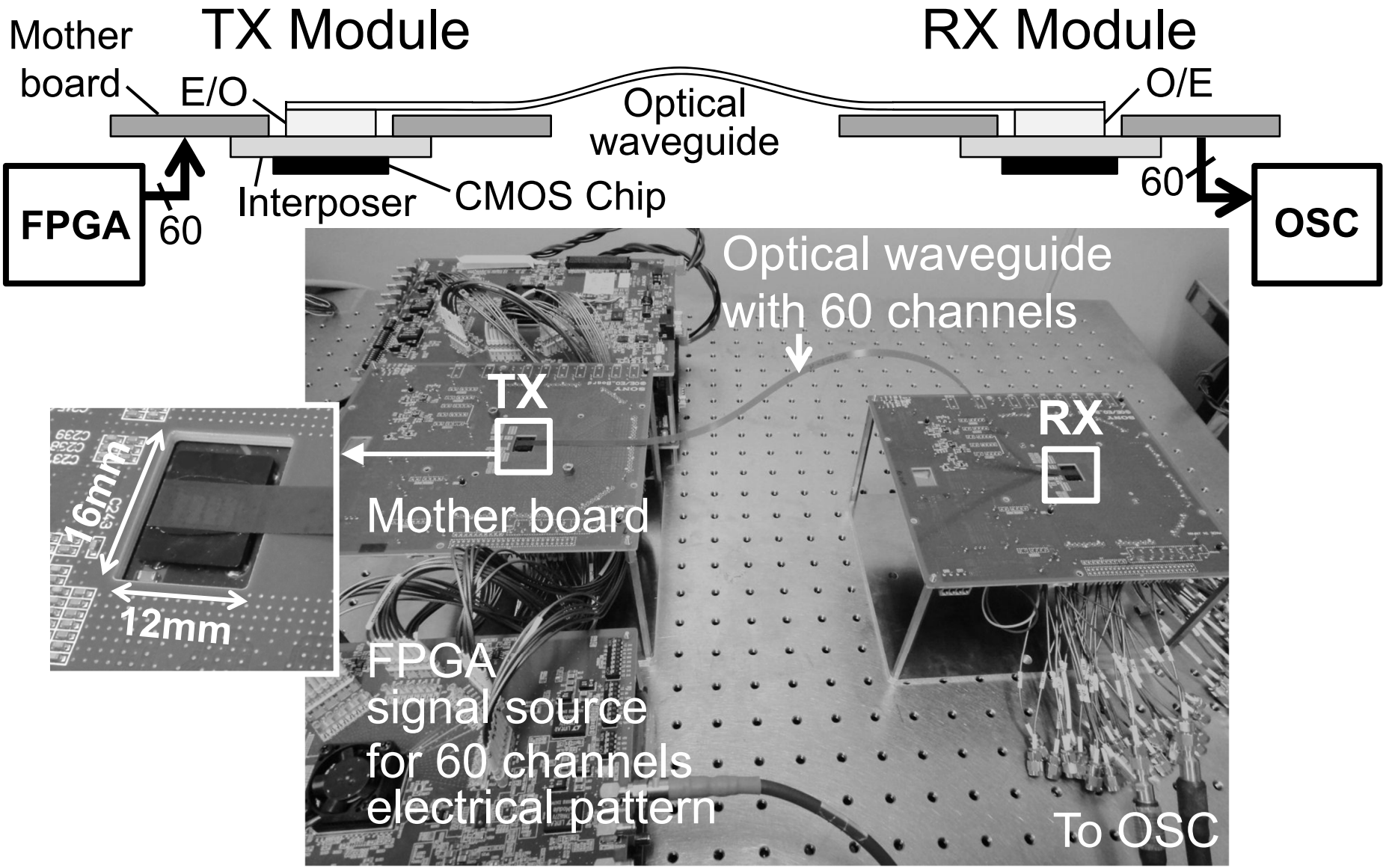
- 10Gb/s 2^7-1 PRBS
- One channel enabled
- Loss of the transmission line de-embedded
- Jitter : $10.89ps_{PP}$
- 9.6mW/ch (TIA block)

Receiver Sensitivity



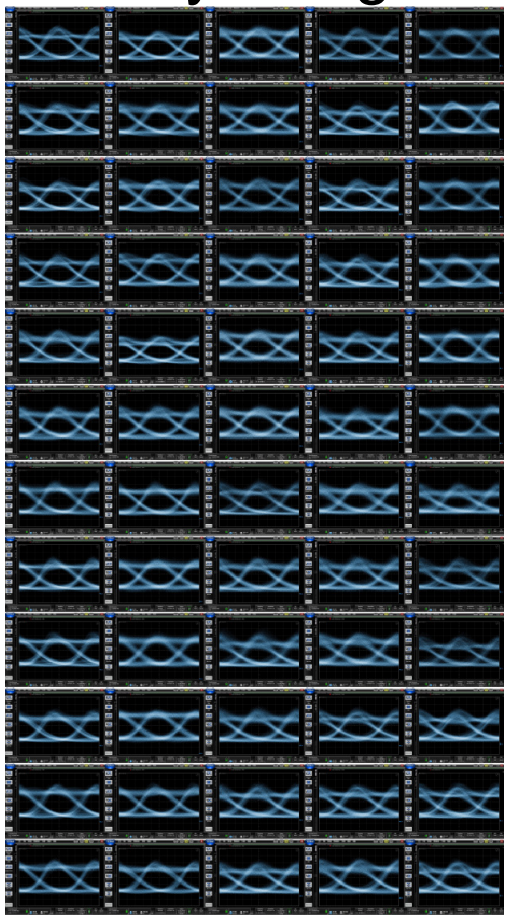
- Input data : 10Gb/s 2^7-1 PRBS
- Input sensitivity : 13.3μA_{PP} @BER = 10^{-12}
- Input referred noise : 0.95μA_{rms}

60ch Measurement Setup



600Gb/s Operation

Optical eye diagrams Electrical eye diagrams



Without de-embedding

- All 60 channels enabled
- BER < 10^{-12} for all 60 channels at 10Gb/s confirmed

Outline

- Motivation
- Architecture
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Performance Results

LDD	
Process technology	CMOS 65nm
Topology	LFD + HFD
Total data rate	600Gb/s
Supply voltage	1.2V, 3.3V
Power dissipation at Ib=7mA, Im=8mA w/o the VCSEL consumption	2.17mW/Gb/s
Area	510um x 250um

TIA	
Process technology	CMOS 65nm
Topology	CMOS Inverter
Total data rate	600Gb/s
Supply voltage	1.6V
Power dissipation	0.96mW/Gb/s
Sensitivity at BER<10^{-12}	13.3uApp
Area	170um x 25um

TIA Comparison

	[3]	[4]	[7]*6	[5]		This work
Process technology	SiGe BiCMOS	CMOS 65nm	CMOS 0.18μm	CMOS 90nm		CMOS 65nm
TIA core topology				T-Coil	CMOS single-ended	CMOS w/ SEDC*1
Number of channels	4	4	12	1	1	60
Data rate (Gb/s)	25	25	10	25	22	10
Total data rate (Gb/s)	100	100	120	25	22	600
Power dissipation (mW/(Gb/s))	2.74	3.64*2	1.80	0.11*3	0.24*2,4	0.96
Sensitivity at BER<10^{-12} (μA_{pp})	47.3	86.0	37.8	55.0*4	43.7*4	13.3
FOM*5	9.46	17.20	11.95	11.00	9.32	4.21
Transimpedance (dBΩ)		76.8	53.0	45.7	45.8	63.2

$$*5: \text{FOM} = \frac{\text{Sensitivity}}{\sqrt{(\text{data rate})}} \ (\mu A/\sqrt{Gb/s})$$

*1 : single-ended-to-differential convertor
*2 : with LA dissipation
*3 : @17.5Gb/s
*4 : @15.0Gb/s
*6 : [7] L. Zhiqqun, et al., "Design of a 12-Channel 120-Gb/s Optical Receiver Front-End Amplifier in 0.18μm CMOS Technology," ***Photonics and Optoelectronic (SOPO), 2010 Symposium***, Jun. 2010.

Summary

- 600Gb/s optical waveguide transmission
  - 65nm standard CMOS process
  - 12 × 5 two dimensional optical I/O array
- LDD: Low power topology
  - HFD + LFD
- TIA: Low noise topology
  - CMOS inverter
  - BW enhancement by positive-feedback

A Power-Scalable 7-Tap FIR Equalizer with Tunable Active Delay Line for 10-to-25Gb/s Multi-Mode Fiber EDC in 28nm LP-CMOS

E. Mammei, F. Loi, F. Radice*, A. Dati*,

M. Bruccoleri*, M. Bassi, A. Mazzanti

Università degli Studi di Pavia, Pavia, Italy

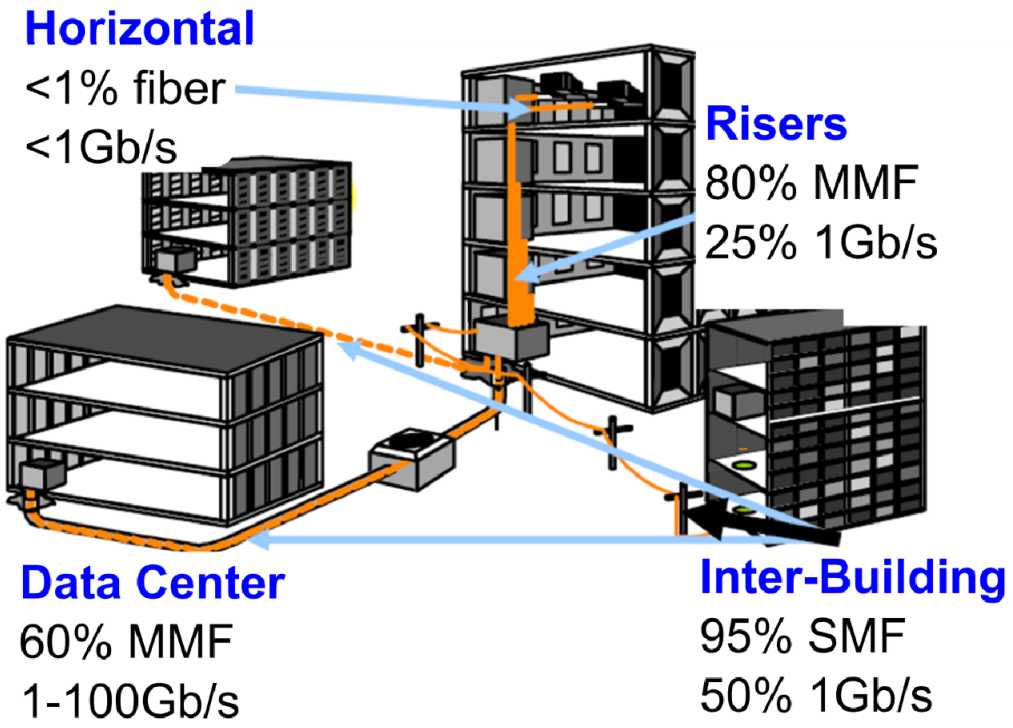
* STMicroelectronics, Cornaredo, Italy

Outline

- **Introduction**
- **FIR Equalizer Design**
  - Analog Delay Line
  - Multipliers
  - Output Stage
- **Experimental results**
  - MMF-emulation setup
  - Summary and comparison
- **Conclusions**

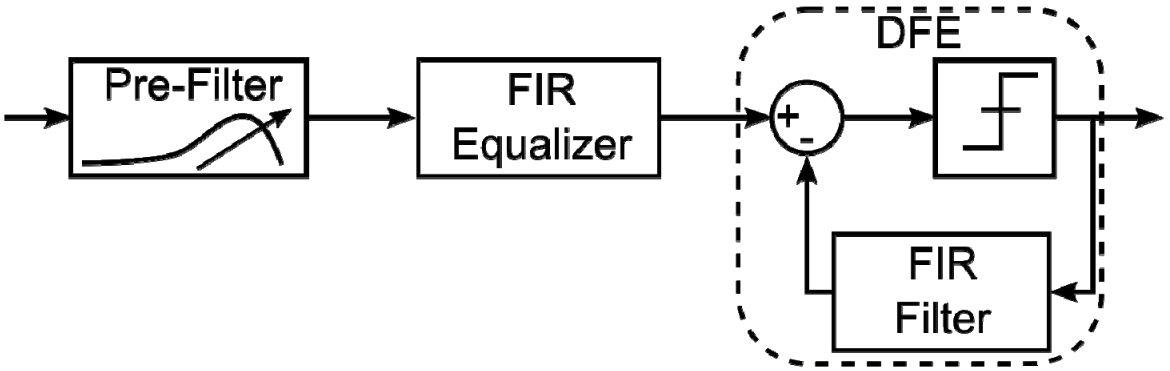
Multi-Mode Fibers LANs

- Data Center is the main MMF market
- New standard foresee 16x25Gb/s with total speed of 400Gb/s



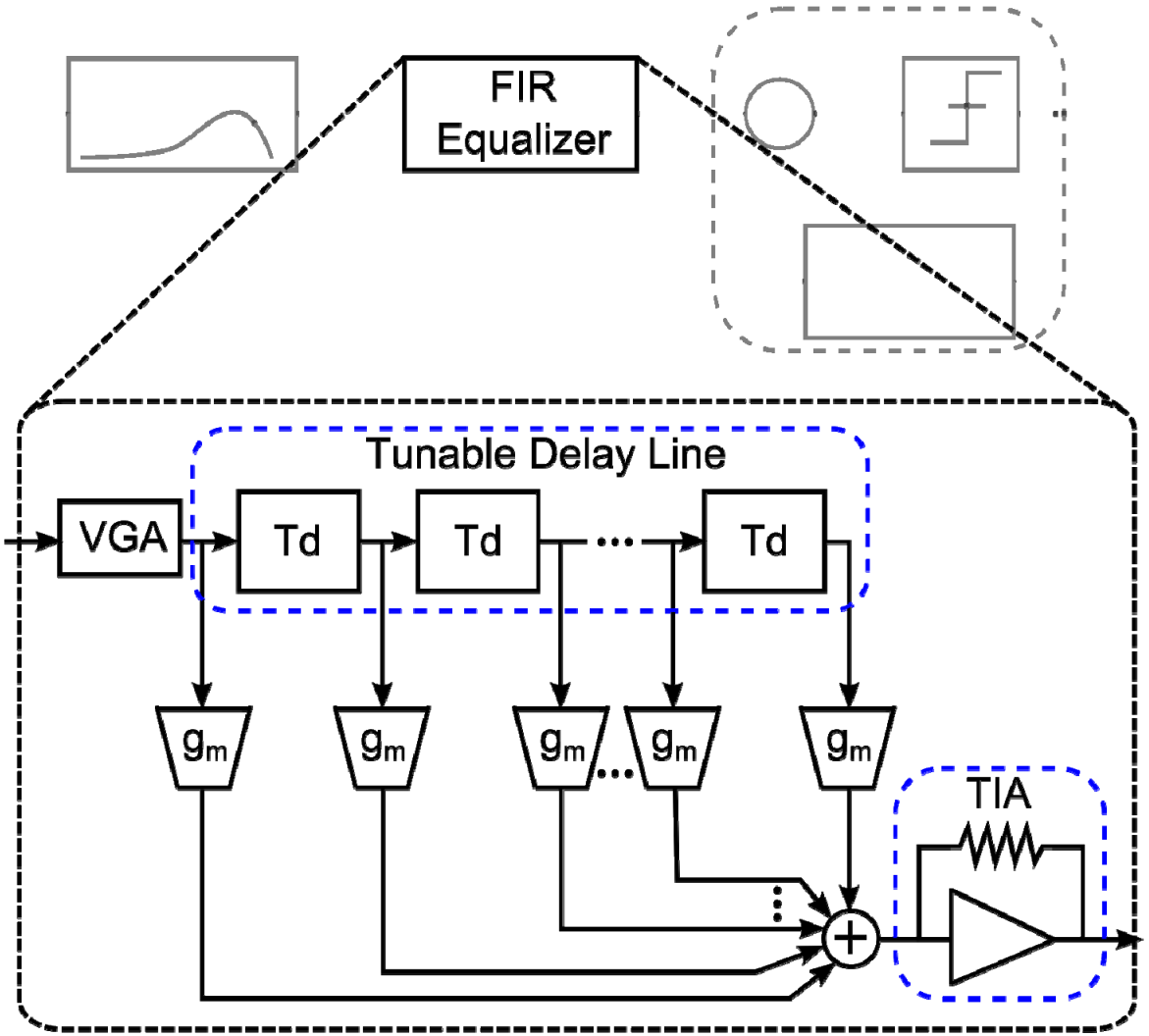
- MMF link capability severely limited by Modal Dispersion
- Electronic Dispersion Compensation (EDC) required

Electronic Dispersion Compensation



- Flexible DSP-based EDCs proposed for 10GBASE-LRM
- Analog EDC more efficient at Data-Rate > 10Gb/s
- Design of analog FIR is challenging:
  - clock generation and distribution issues with sampled time delay lines
  - large area and low tuning range with continuous time LC delay lines

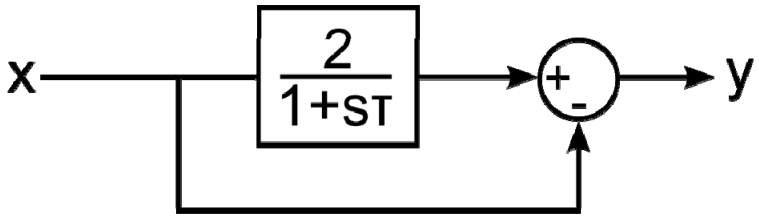
FIR Equalizer Block Diagram



Proposed FIR:

- Compact 7-TAPs active tunable delay
- 10 to 25Gb/s with scalable power dissipation
- CMOS 28nm LP

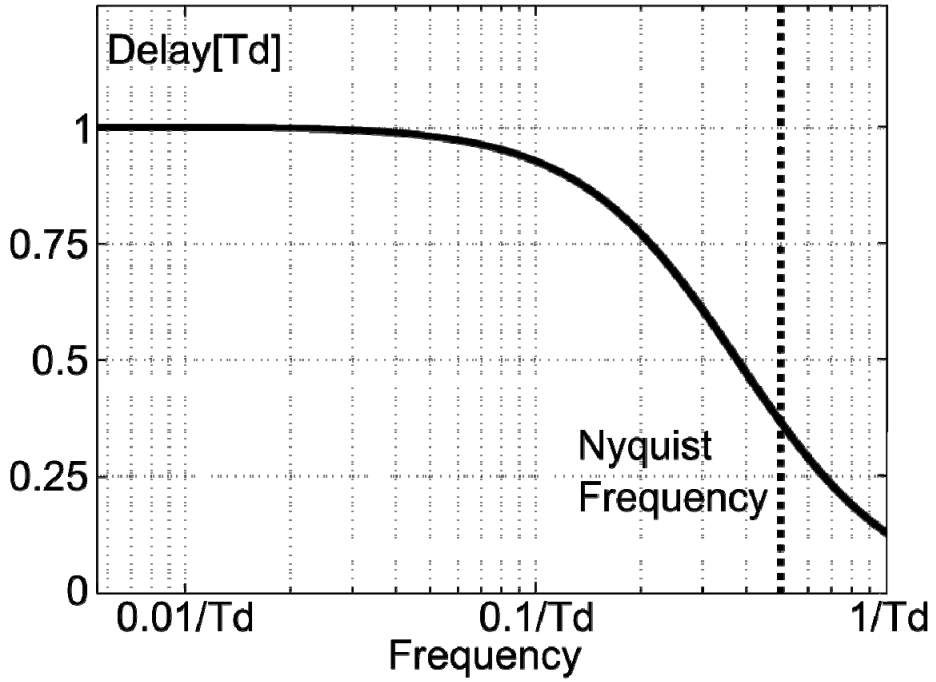
Analog Delay: First Order All-Pass Filter



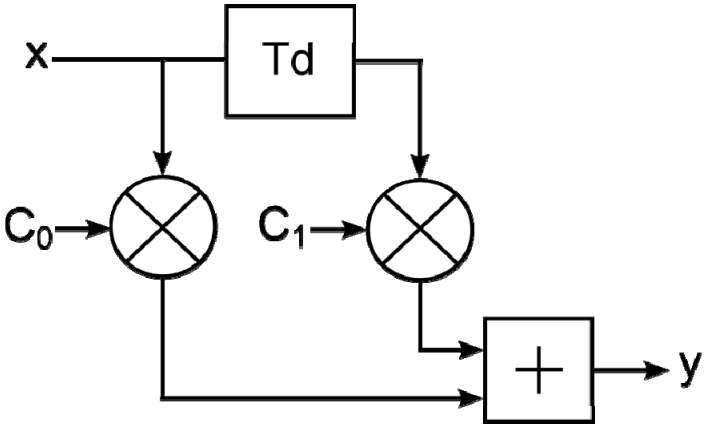
$$y(s) = \frac{2}{1+s\tau} - 1 = \frac{1-s\tau}{1+s\tau}$$

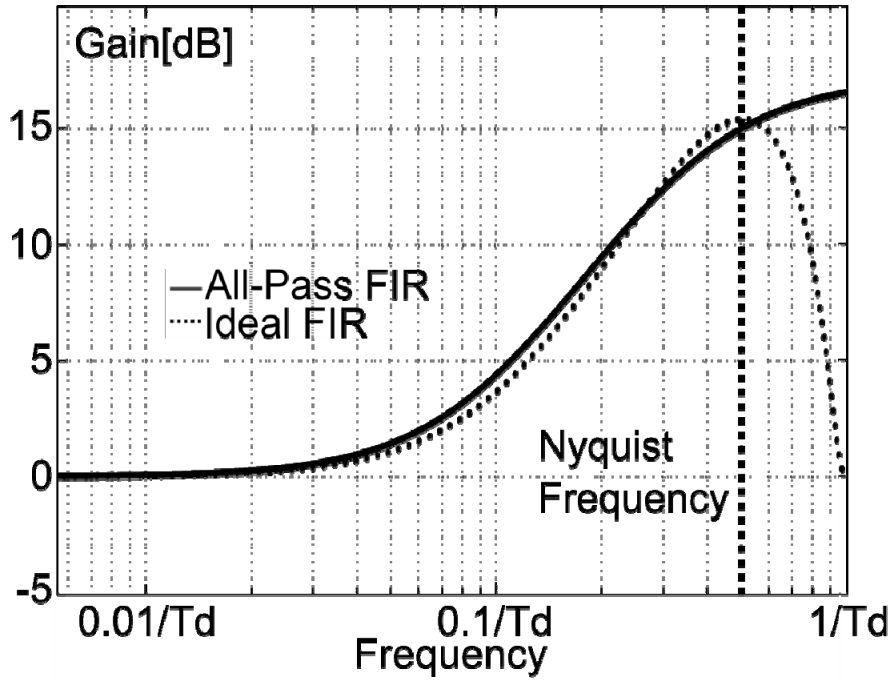
$$G.D. = -\frac{\partial\varphi}{\partial\omega} = \frac{2\tau}{1+(\omega\tau)^2}$$

- Bandwidth independent from delay
- Variable delay by tuning the pole time constant
- Group delay roll-off is not an issue



Effect of the Group-Delay Roll-Off

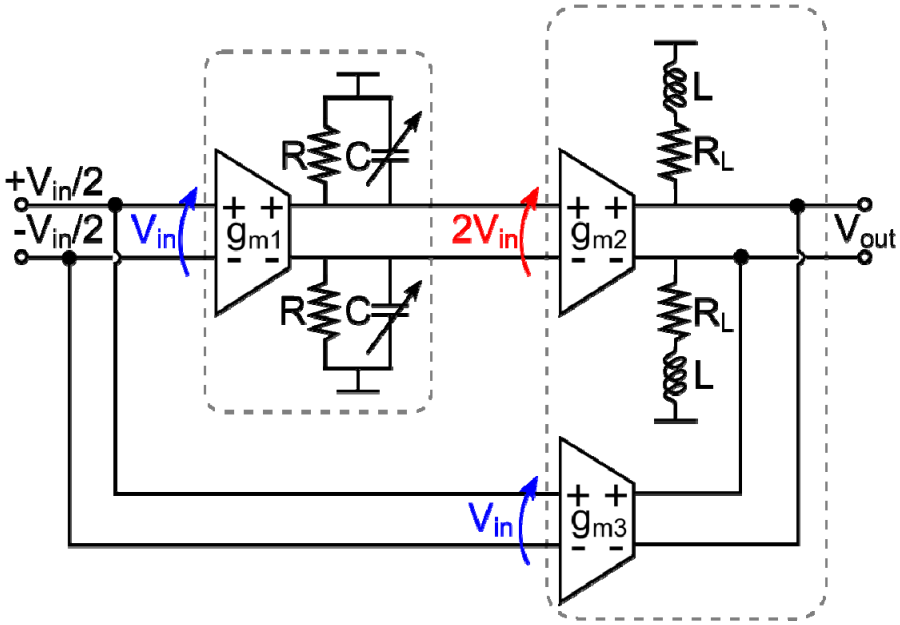




Example: 2TAP FIR filter with 15dB boost @ Nyquist freq.

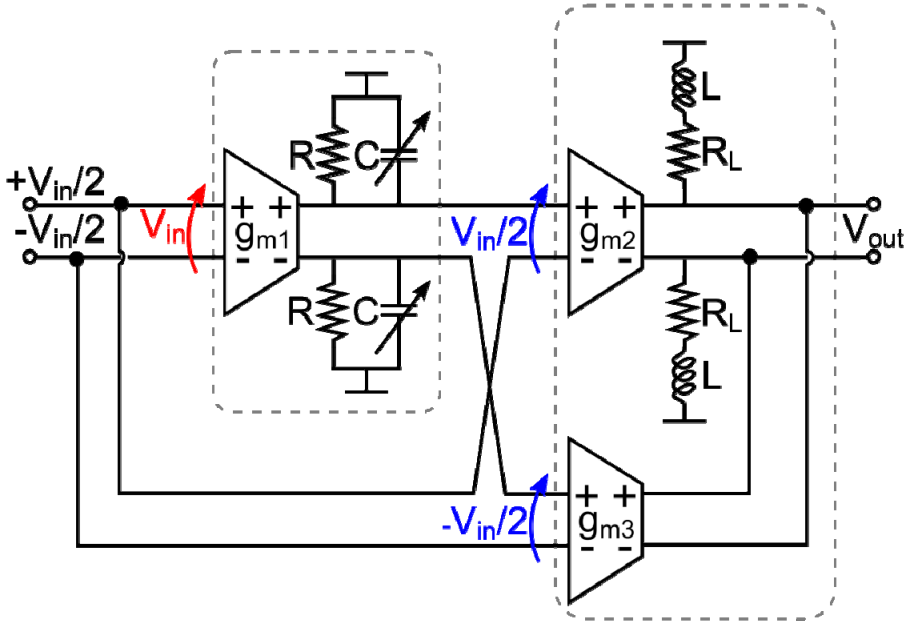
- Ideal delay: C_0=3.3, C_1=-2.3
- All-Pass: C_0=3.8, C_1=-2.8
- Ideal FIR transfer function is "folded" around Nyquist
- FIR with all-pass delay has similar in-band shape and boost above Nyquist

Analog Delay: Circuit Realization



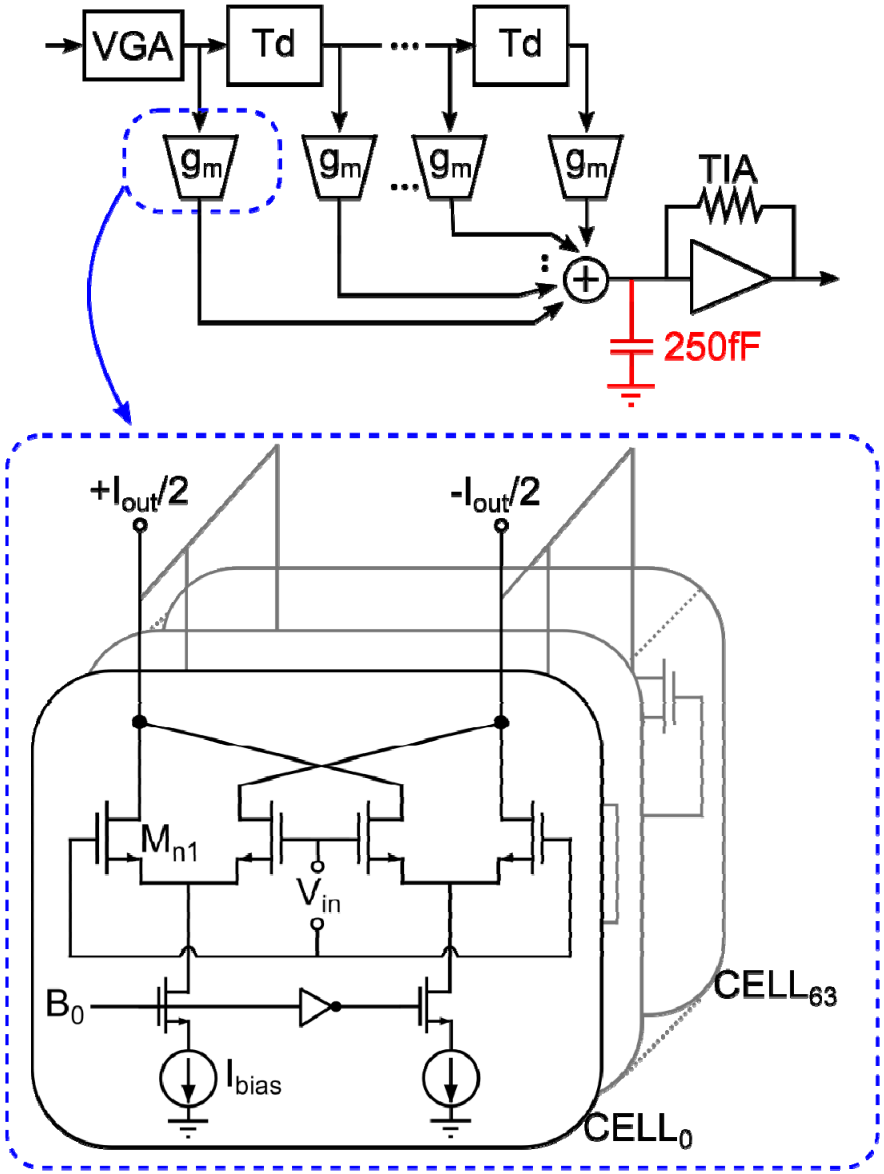
- g_{m1} and the RC load form the programmable lowpass filter
- g_{m2} and g_{m3} are used to subtract input signals
- g_{m2} has maximum input swing ($2V_{in}$) and limits linearity

Analog Delay: Circuit Realization



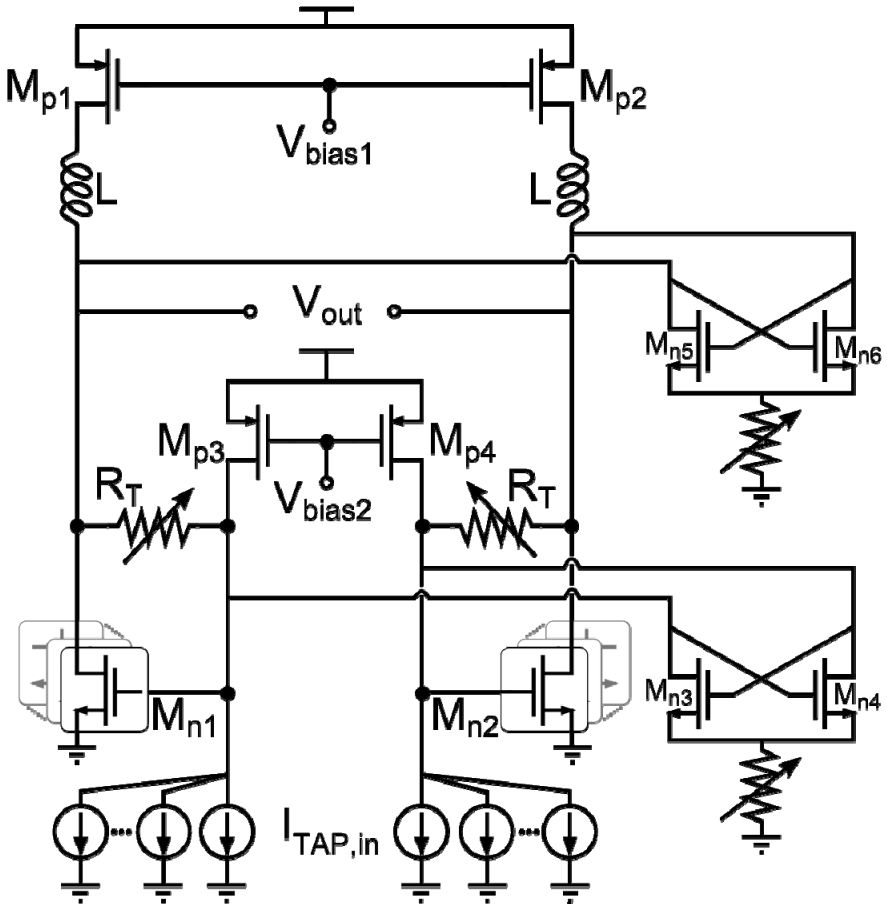
- Maximum now on g_{m1} limited to V_{in}
- 1dB C.P ~220mV 0-pk diff (~ +6dB)
- Programmable group delay from 30 to 75ps

Taps: Programmable Transconductors



- Resolution: 6BIT thermometric
- Very large capacitance (~250fF) on the summing node
- Transimpedance amplifier used for summing output currents

Trans-Impedance Amplifier



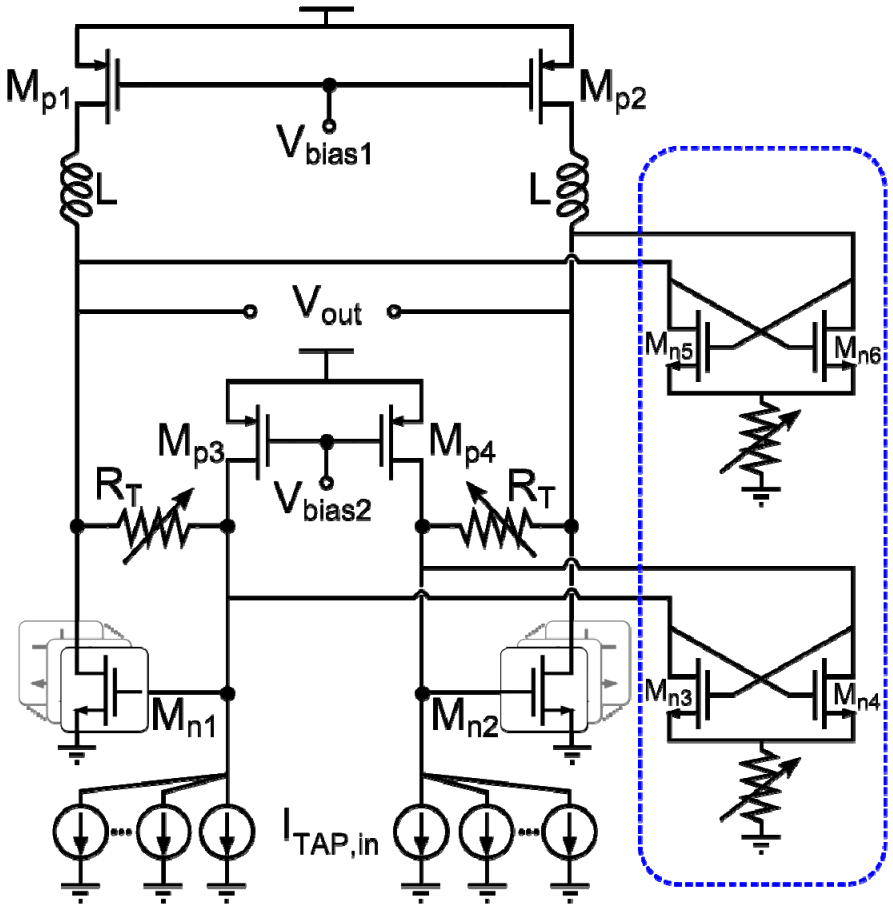
- Common source topology with peaking inductors
- Programmable bandwidth, gain and dissipation
- Low MOS gain (g_m/g_{ds}~5) impairs performances

Slide 11

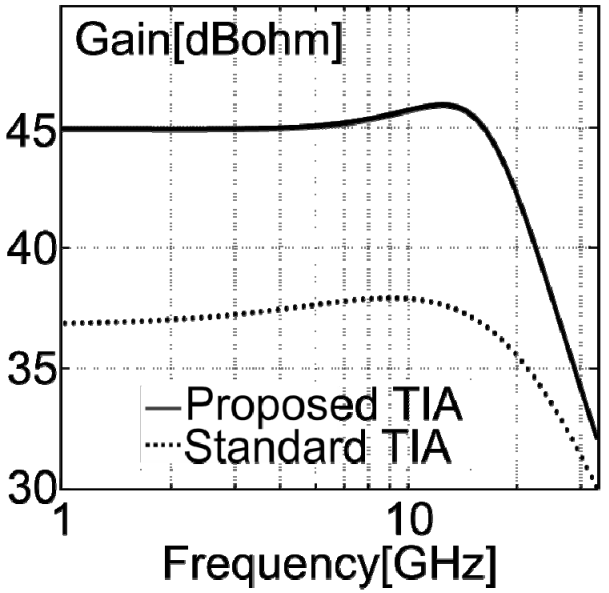
F3 Evidenzierei con una caption qual è la misura e quale la simulazione

Frank, 1/19/2013

Trans-Impedance Amplifier



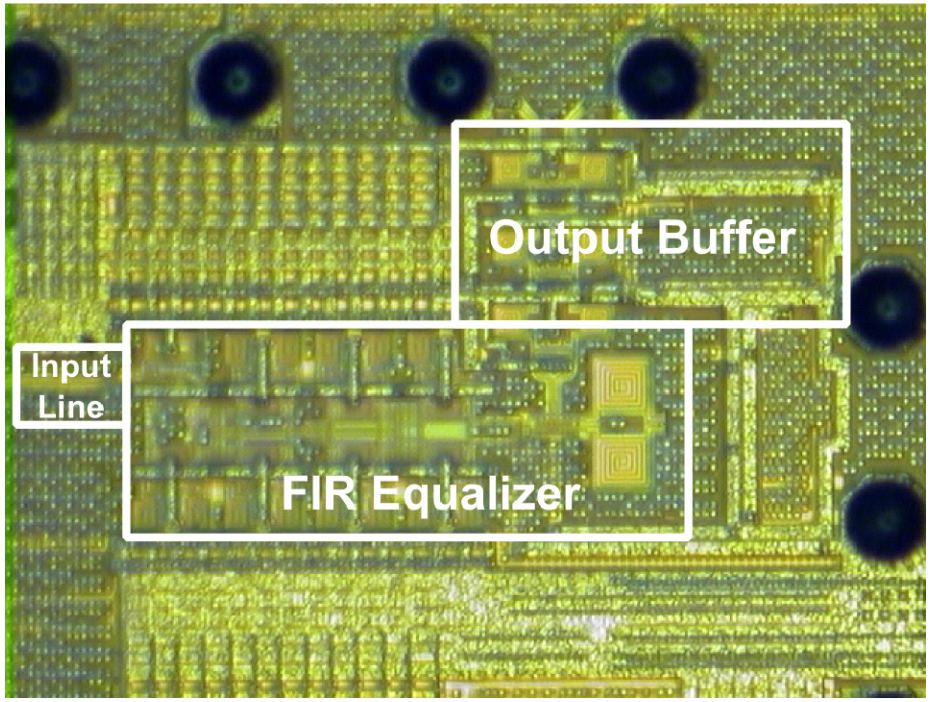
- Negative R to cancel output conductances
- 2.5x trans-resistance
- 0.5x input noise



F4 Evidenzierei con una caption qual è la misura e quale la simulazione

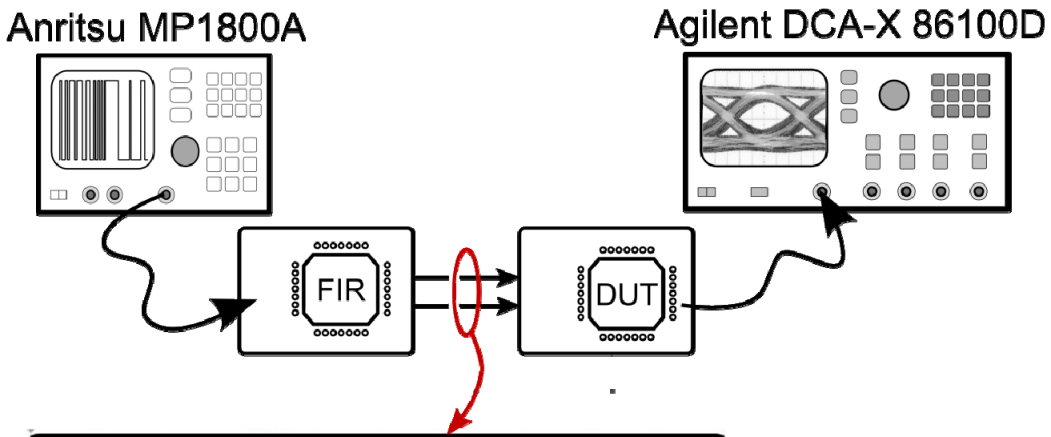
Frank, 1/19/2013

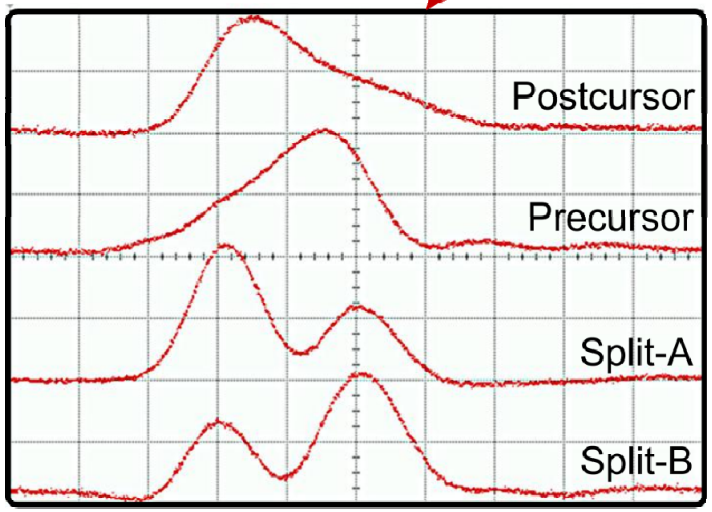
Test Chip



- 10ML CMOS 28nm LP from STMicroelectronics
- Core area: 0.085mm^2
- Supply Voltage:1V
- Data rate: 10 to 25Gb/s
- Power: 55 to 90mW
  - 5.5 to 9mW Delay
  - 10 to 25mW TIA
  - 7x1.5mW Multipliers

MMF Link Emulation Setup

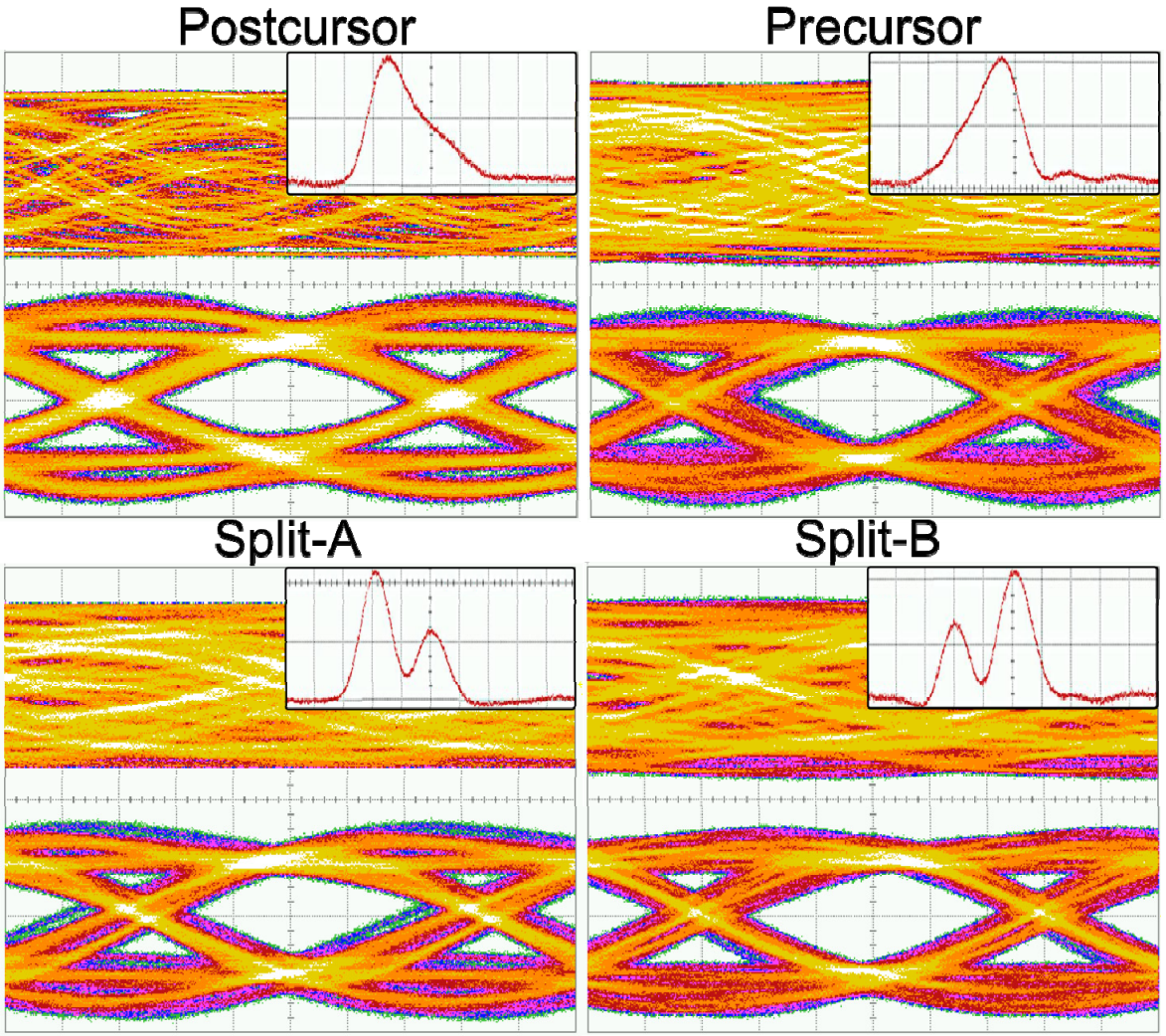




Pulse responses spread over 4-5 symbol periods

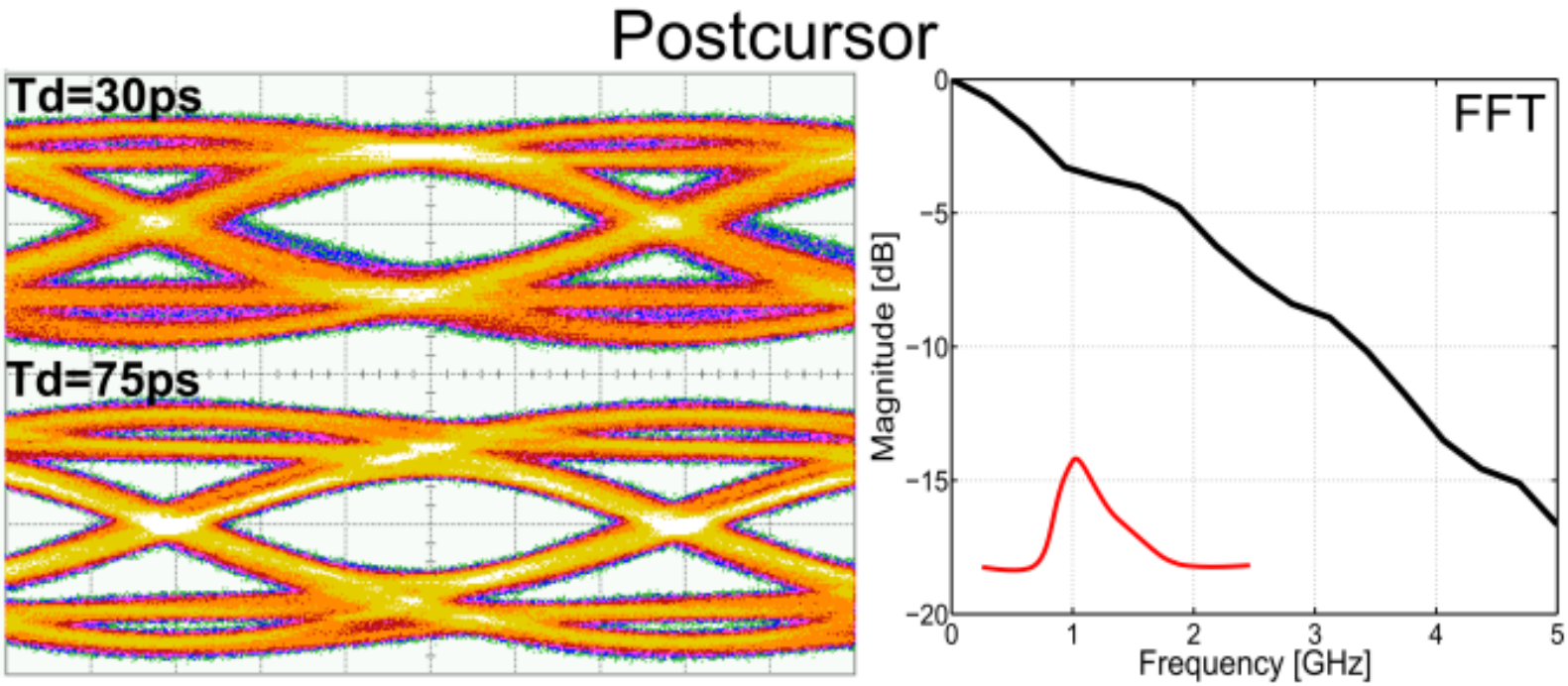
- First chip emulates MMF pulse response
- A second chip (DUT) performs equalization
- Output connected to a sampling scope
- Coefficients adapted with a PC running an adaptation algorithm

25Gbps Eye Diagram Measurements



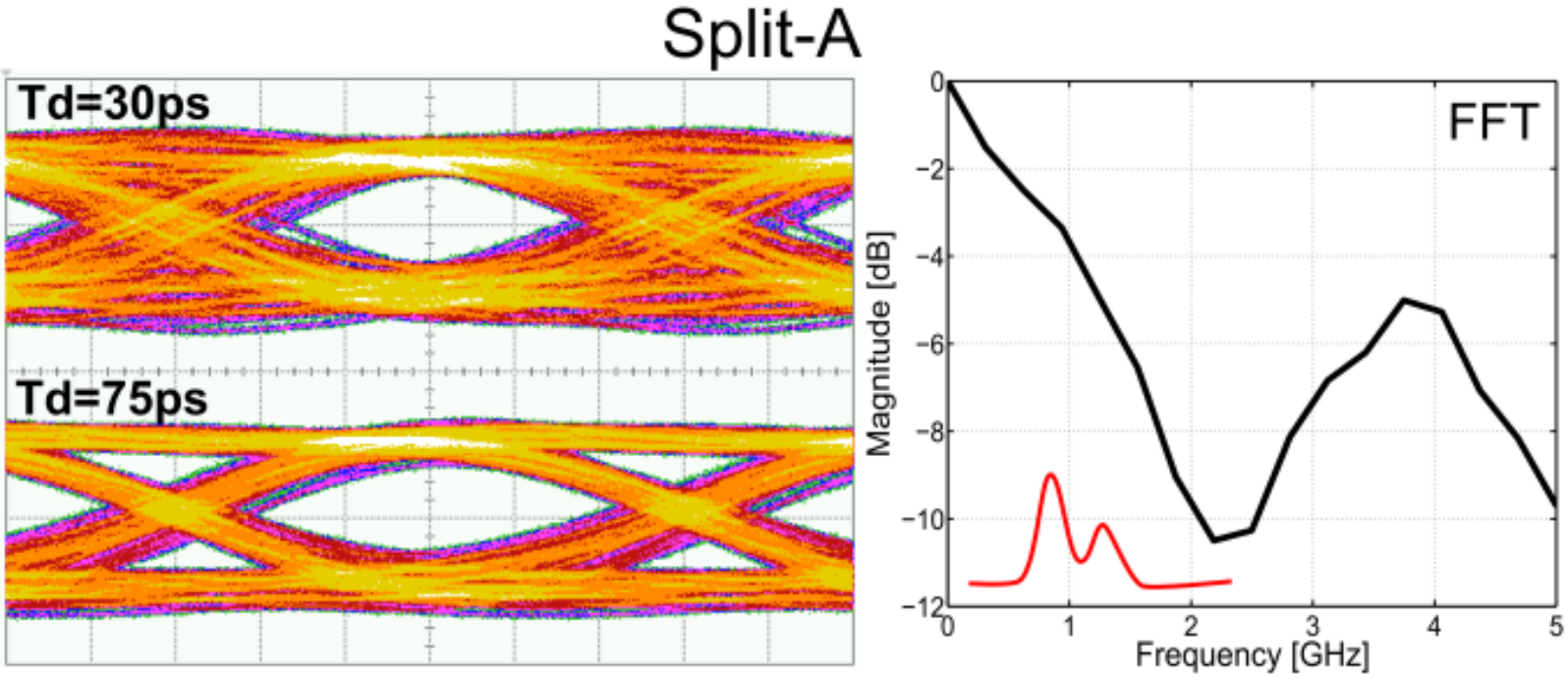
- Td=3/4 Tbit (30ps)
- H. and V. openings better than 43% and 57%
- ~100mV vertical amplitude
- Integrated output noise <4mV$_{rms}$

Eye Diagram at 10Gbps: Postcursor



- "Postcursor" channel has a fairly regular low-pass shape
- Can be equalized with a simple high-pass response
- **Adjusting Td gives minor performance improvement**

Eye Diagram at 10Gbps: Split-A



- "Split-A" channel has ad in-band notch
- Setting a larger Td shifts the FIR equalizing capability to lower frequency
- **Increasing Td improves H. opening from 48% to 69%**

Summary and comparison

Ref.	Tech.	Data Rate [Gb/s]	# Taps	Total Delay [ps]	Power [mW]	Power / (DataRate•TotalDelay) [mW]	Core Area* [mm^2]
Wu JSSC 2003	180n SiGe	10	7	300	40	13.3	1.9
Reynolds ISSCC 2005	130n CMOS	10	7	450	325	72.2	3.8
Sewter JSSC 2006	90n CMOS	24 - 30	3	70	25	14.8 - 11.9	0.3
Sewter JSSC 2006	180n CMOS	30 - 40	3	50	70	46.6 - 35	0.45
Momtaz JSSC 2010	65n CMOS	40	7	75	65	21.6	0.75
This Work	**28n CMOS**	**10 - 25**	**7**	**450 - 180**	**55 - 90**	**12.2 - 20**	**0.085**

* Estimated from chip micrograph

Conclusions

- A continuous-time analog FIR equalizer for next generation MMF links at 25Gb/s, has been presented
- Active all-pass sections are proposed to realize a very compact 7-taps continuous time delay line showing large tuning-range and scalable dissipation
- Measurements on a 28nm LP-CMOS test-chip prove data equalization with channel responses typical of MMF and show the importance of having a tunable delay line to keep optimal performance at different data rate.

A 28Gb/s 1pJ/b Shared-Inductor Optical Receiver with 56% Chip-Area Reduction in 28nm CMOS

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Ming-Chieh Huang[1], Chih-Chang Lin[1],and Fu-Lung Hsueh[3]

[1] TSMC Design Center, San Jose, CA
[2] nVidia, San Jose, CA
[3] TSMC, Hsinchu, Taiwan

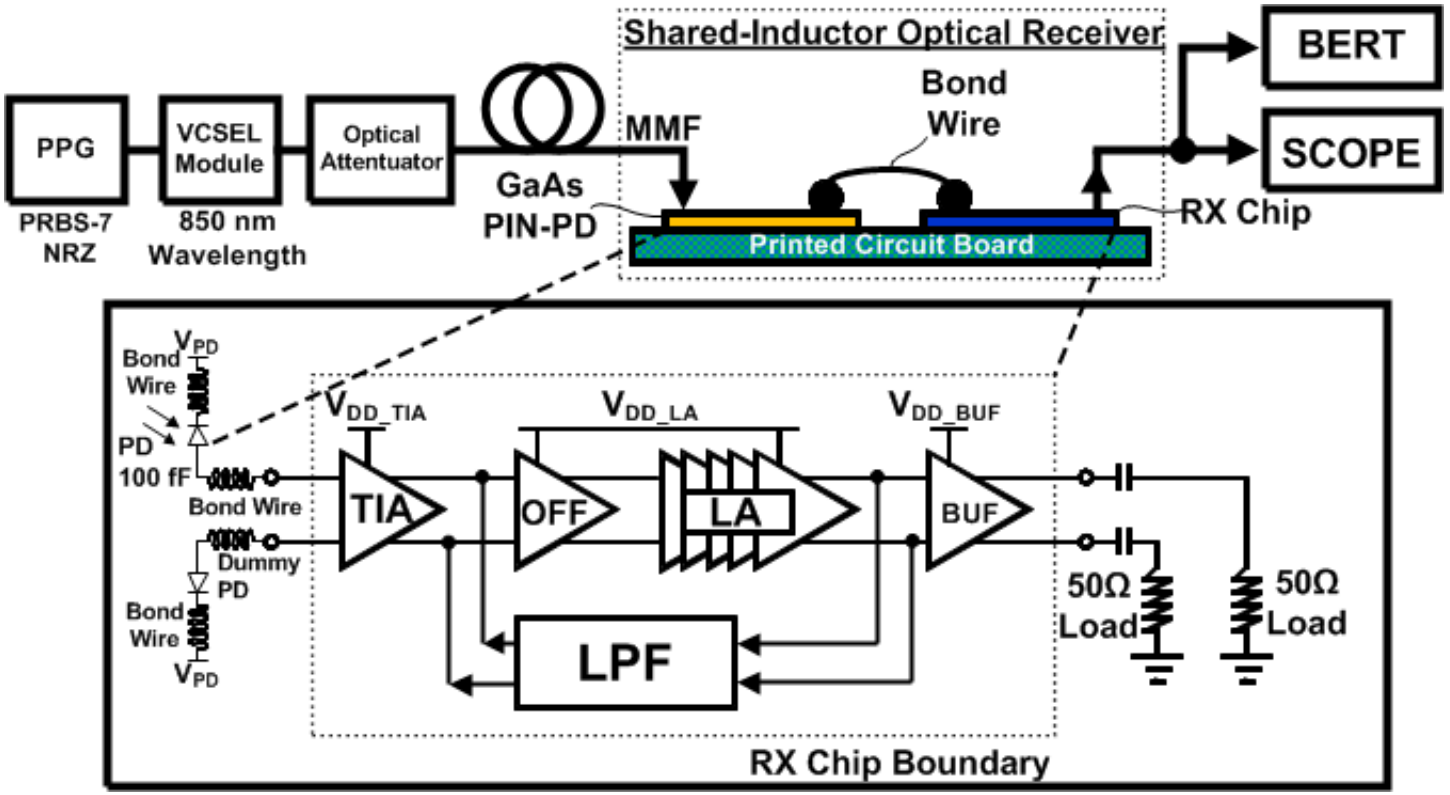
Outline

- Motivation
- Receiver architecture
  - Pseudo-differential CMOS push-pull TIA
  - Conventional and Shared-Inductor LA
- Measurement results
  - Conventional RX v.s. Shared-Inductor RX
- Summary

Motivation

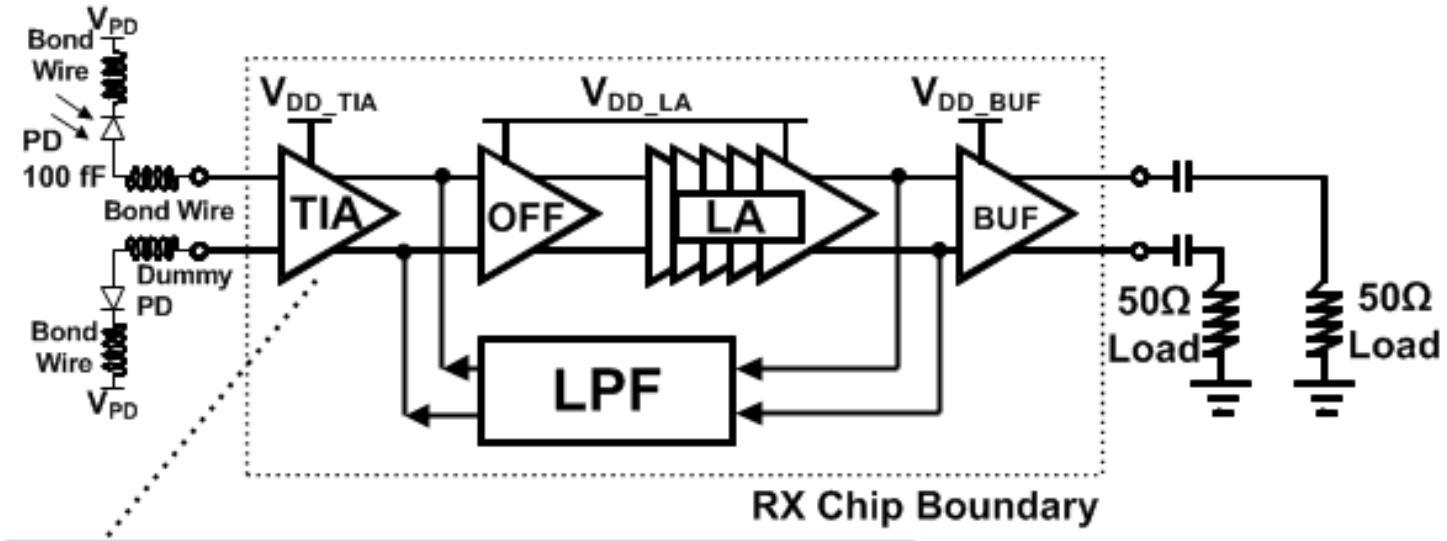
- Optical interconnect is promising for energy-efficient high-speed serial-link
- Inductive-peaking is a common technique for high-speed transceivers to boost circuit bandwidth at the cost of the chip area
- In this work, we demonstrate by sharing inductors in 28nm CMOS optical receiver, the chip area can be reduced by 56% without sacrificing energy-efficiency or data rates

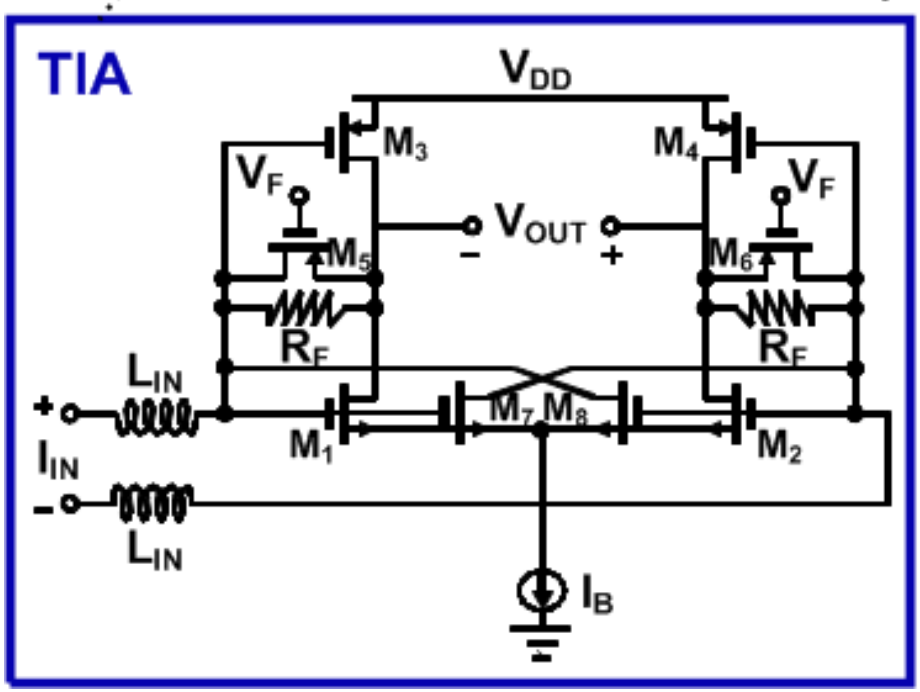
CMOS RX with Off-Chip Photodiode



- Two optical RXs on the same die with different LA designs
- 850nm Vertical Cavity Surface Emitting Laser (VCSEL) as the light source and 100fF photodiode (PD) wire-bonded to RX
- 2m-long 50μm-diameter multimode fiber (MMF)

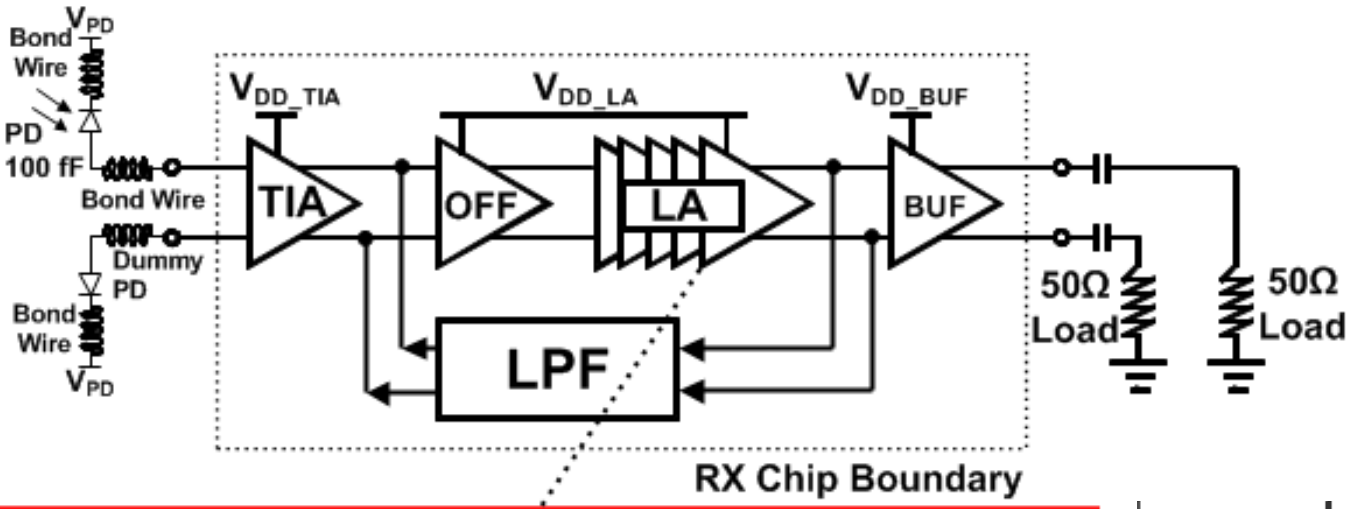
Pseudo-Differential CMOS Push-Pull TIA

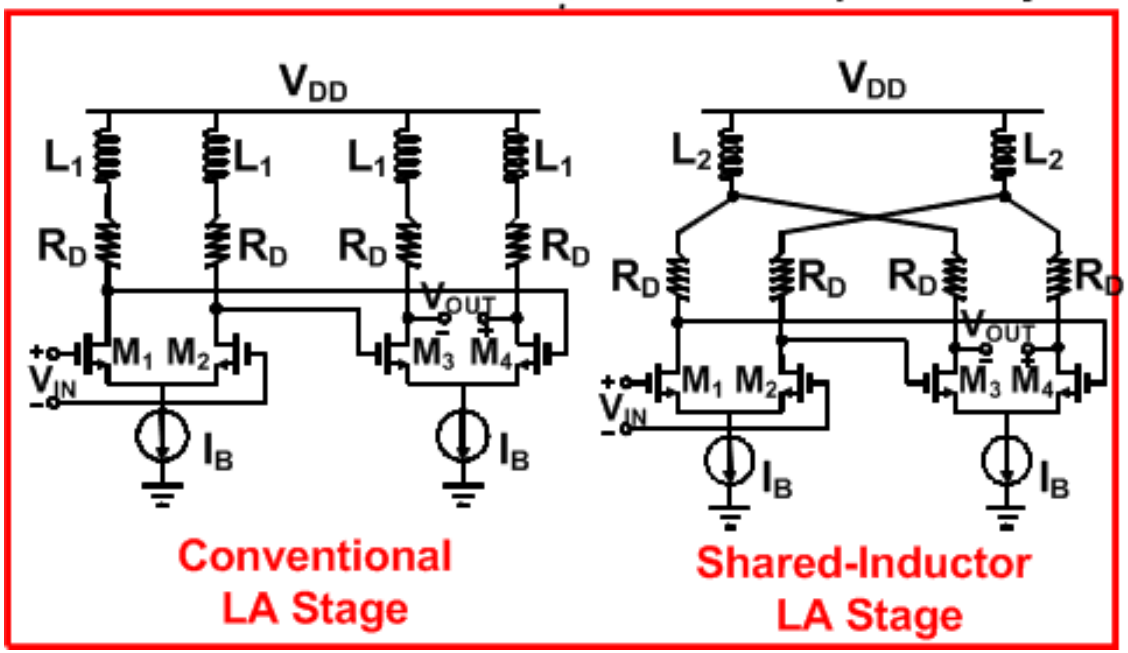




- CMOS TIA provides high gain and low-power but is sensitive to supply noises
- I_B dictates *gm* of M_1 ~ M_4 and makes TIA less-sensitive to supply noises
- M_7 - M_8 improves single-ended to differential conv

Conventional v.s. Shared-Inductor LA

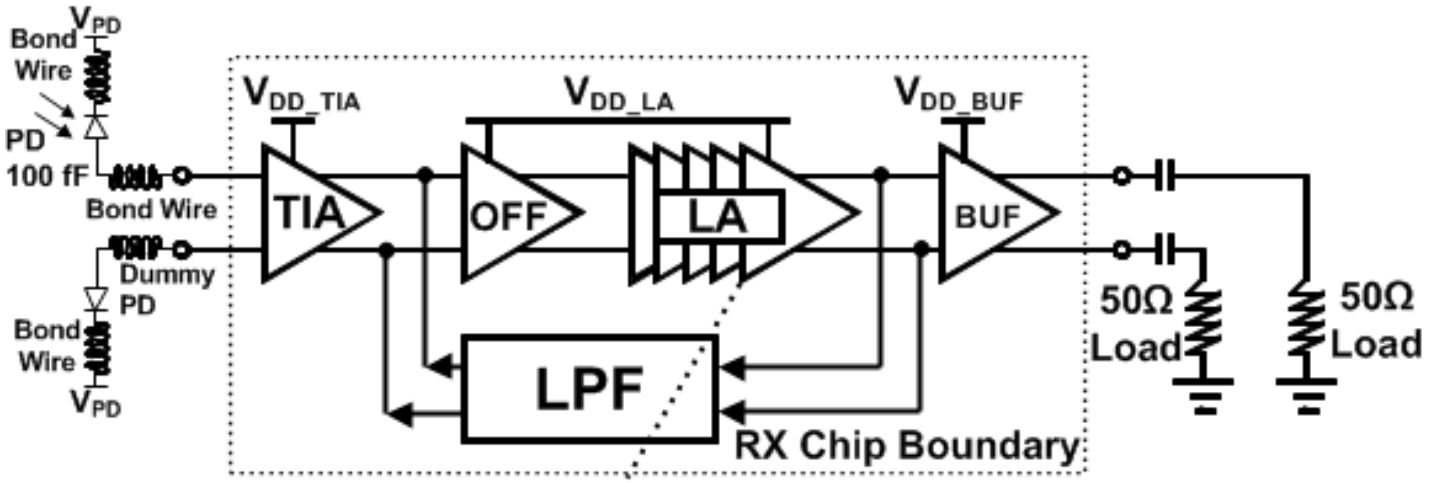


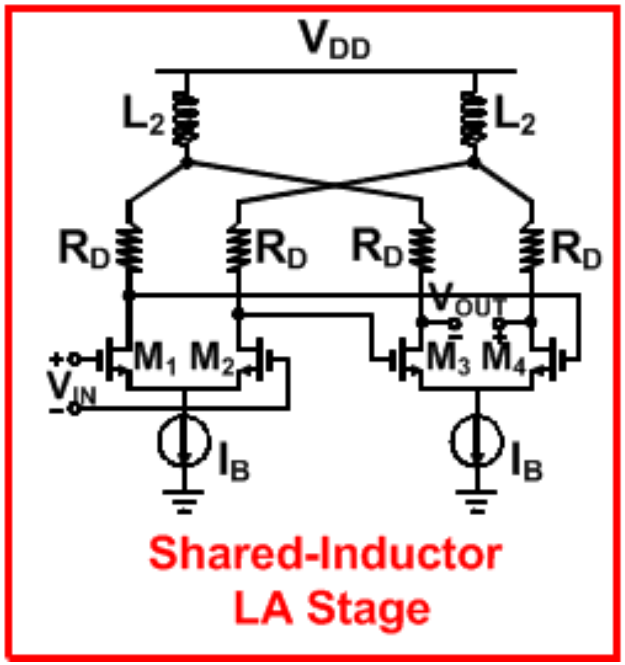


Transfer Function	Main Pole
Conventional	$\frac{\sqrt{R_D^2C_L^2 - 4L_1C_L} + R_DC_L}{2L_1C_L}$
Shared-Inductor	$\frac{\sqrt{R_D^2C_L^2 - 8L_2C_L} + R_DC_L}{4L_2C_L}$

$L_2 = 0.5 * L_1$. Same main pole and zero locations for both LAs;BW~19GHz

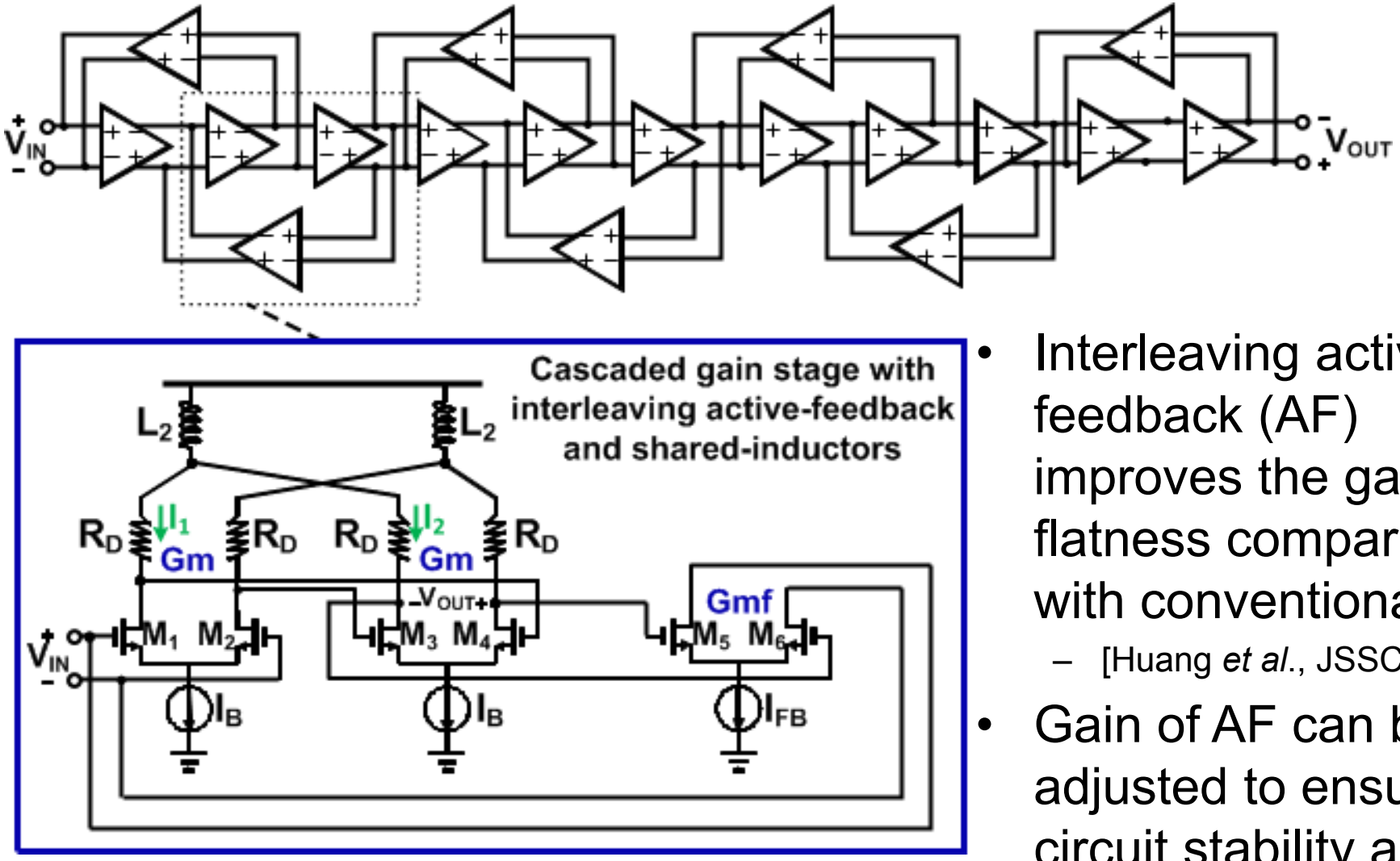
Design Concerns of Shared-Inductor LA





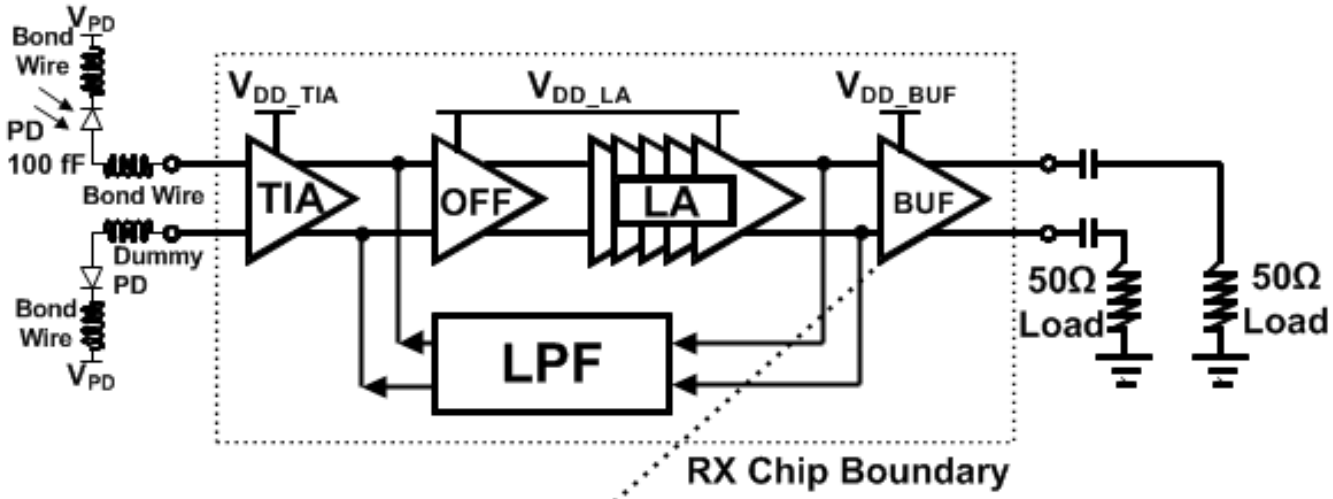
- The active-area of LA can be reduced by >60% with same GBW but the layout matching between M_1-M_3 and M_2-M_4 paths is critical
- Aluminum-RDL layer (1P10M) in 28nm HPM is used for signal routing in-between inductors for low parasitic resistance

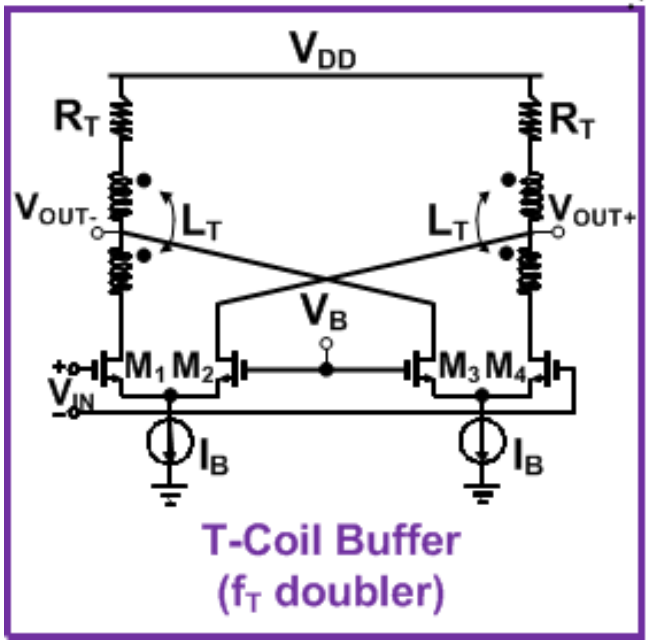
Third-Order Interleaving Active-Feedback



- Interleaving active-feedback (AF) improves the gain flatness compared with conventional AF
  - [Huang *et al.*, JSSC, 5/07]
- Gain of AF can be adjusted to ensure circuit stability across PVT variations

T-Coil f_T-Doubler for Test Buffer

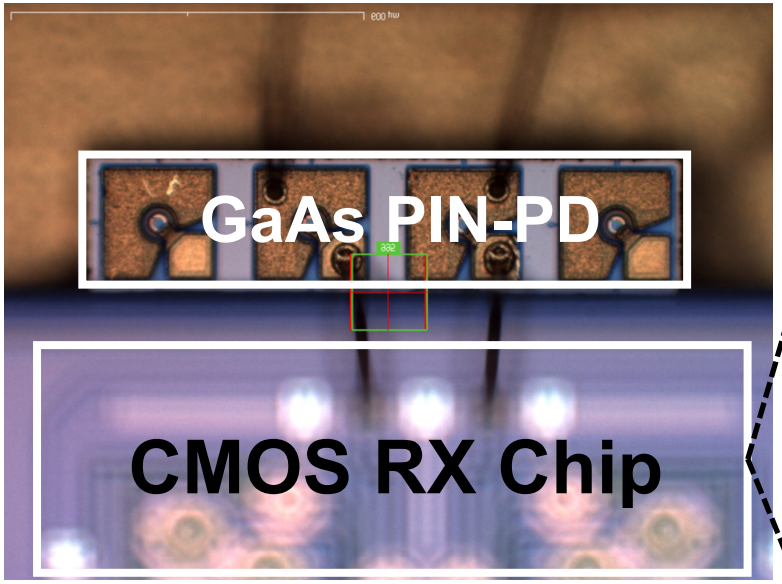




- 50-Ω termination for instrument requires large device sizes M_1 ~ M_4 for sufficient voltage swings
- f_T-doubler reduces input capacitance C_{GS} by half for improving BW
- T-Coils implemented as center-tapped inductors are incorporated to resonate the output load capacitance

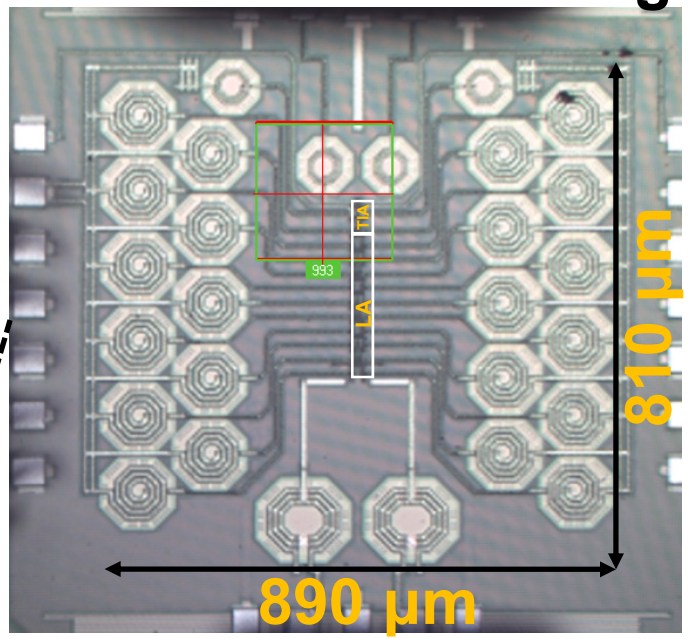
Die Microphotograph (28nm HPM)

CMOS RX chip with wire-bonded off-chip PD

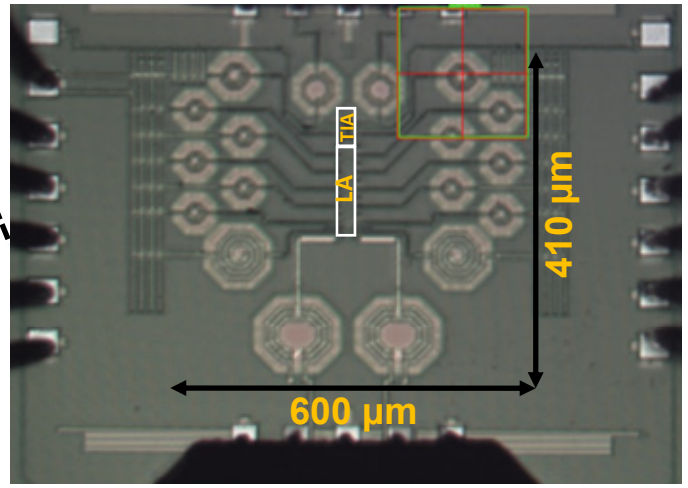


- Active-area is reduced by 56% with test buffer and routing is reduced by 30% due to smaller inductors

Conventional Peaking

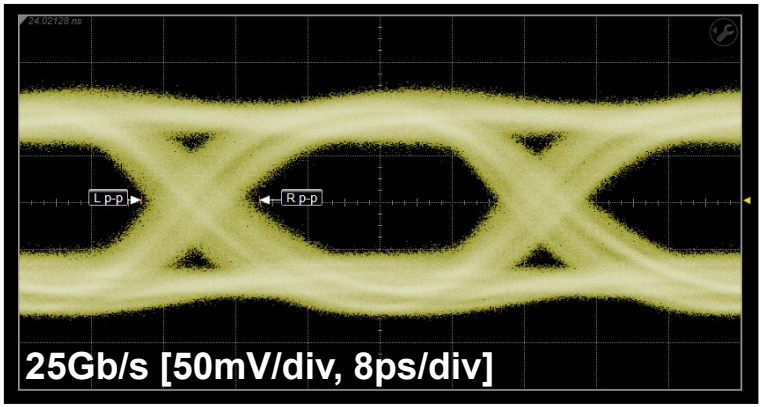


Shared-Inductor

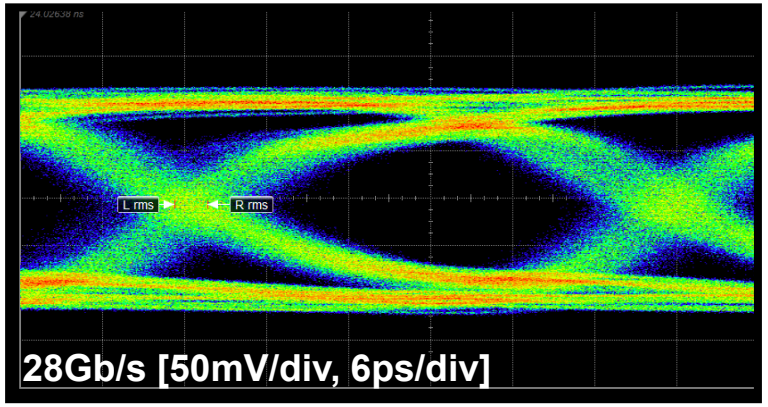


Comparison of Measured Eye Diagrams

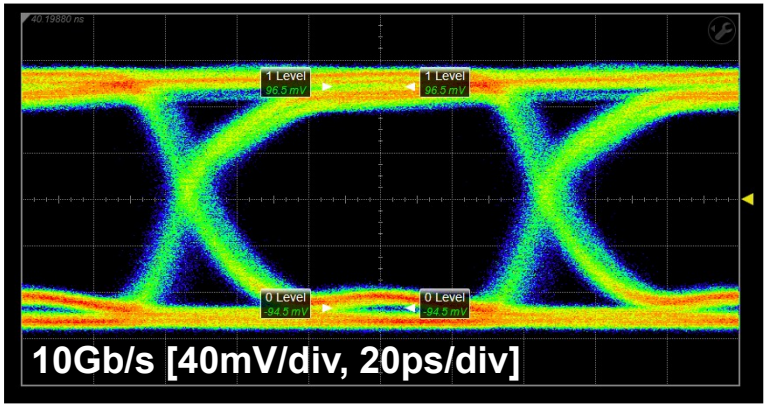
Conventional (400μA$_{PP}$ Electrical)



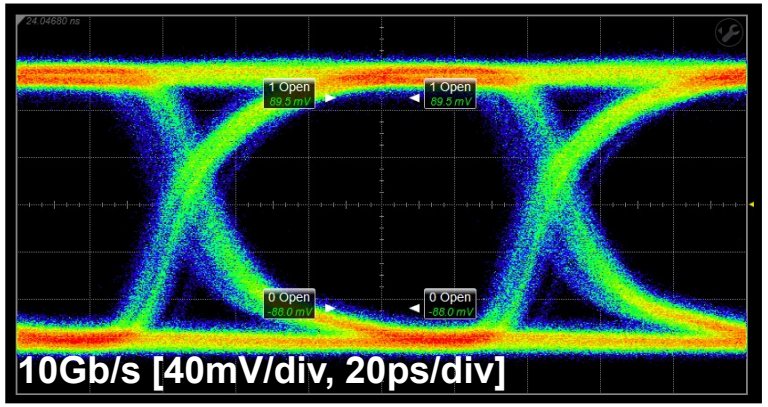
Shared-Inductor (400μA$_{PP}$ Electrical)



Conventional (-6dBm Optical)

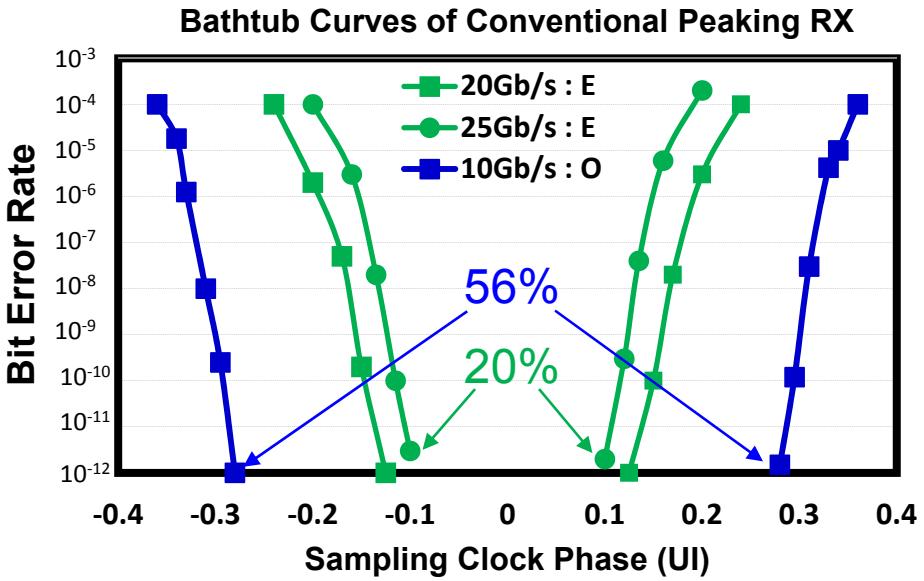


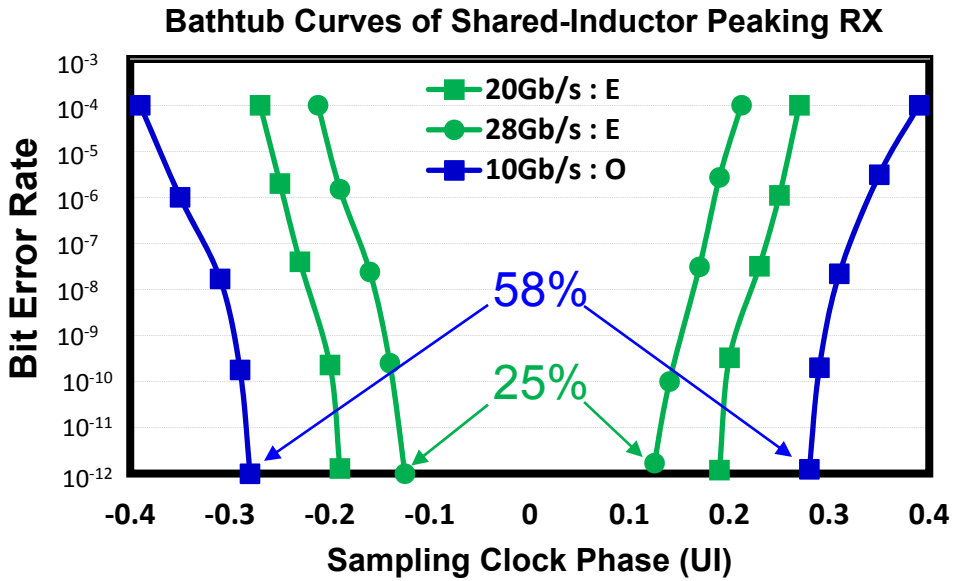
Shared-Inductor (-6dBm Optical)



- 10Gb/s optical eye diagrams show comparable RMS jitter
- Conventional RX up to 25Gb/s for BER<10^{-12}; shared-inductor RX on the same die up to 28Gb/s for BER<10^{-12}

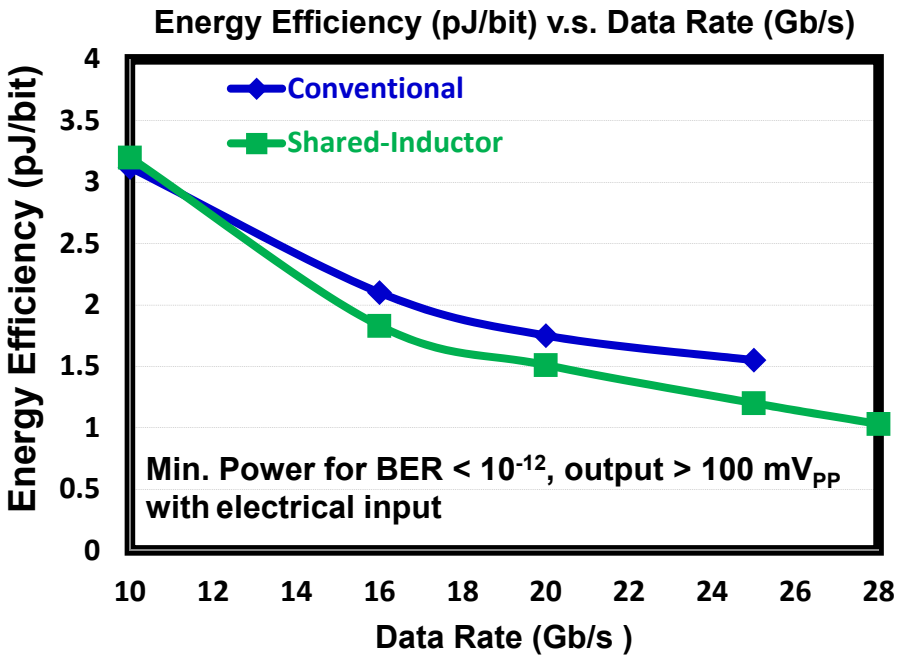
Comparison of Measured Bathtub Curves

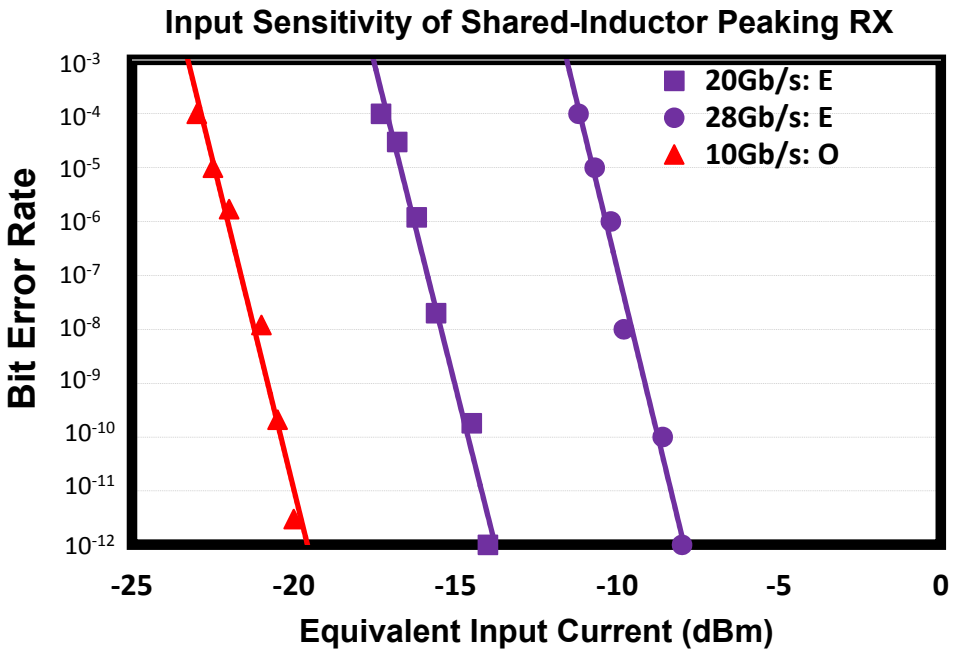




- PRBS7 test patterns for both electrical and optical inputs
  - 400 µA electrical current and -6dBm optical power from VCSEL
- Eye openings of shared-inductor RX reveal better jitter performance and BW because of smaller layout paracitics
  - ISI observed > 20Gb/s for both RXs; no equalizer included
- Speed of optical test is limited by the light source (850nm VCSEL module) that is directly driven by pattern generator

Sensitivity & Efficiency of Shared-Inductor RX





- Optimize energy-efficiency by lowering supply voltages and bias currents while maintaining BER<10^{-12} & >100mV_{PP} swing
- Power penalty for lower speed due to cascaded LA gain stages designed for BW; efficiency improves at higher speeds
- Optical power converted to equivalent electrical current using 0.4A/W responsivity for input sensitivity comparison

Technical Summary of 25-28Gb/s Optical RX

Reference	Data Rate (Gb/s)	Power (mW/ channel)	Energy Efficiency (pJ/bit)	Sensitivity @ 10^{-12} BER (dBm)	PD Cap (fF)	Chip Area (mm^2)	Tech-nology
This work (w/ shared-inductor)	28	28.8*	1.03*	-6 @ 10Gb/s (O) -7 @ 28Gb/s (E)	100	0.6 x 0.53	28nm CMOS
This work (w/o shared-inductor)	25	38.8*	1.55*	-6 @ 10Gb/s (O) -7 @ 25Gb/s (E)	100	0.89 x 0.81	28nm CMOS
[1] ISSCC'13	25	69*	2.76*	-6.8	50	1.6 x 0.65***	65nm CMOS
[2] ISSCC'13	25	67.5 (TIA)	2.7 (TIA)	-12	65	3.3 x 1.5***	130nm SiGe
[3] ISSCC'13	28	137.5**	4.9**	-9.7 @ 25Gb/s	—	2.66 x 2.28***	65nm CMOS
[4] ISSCC'12	25	33.6*/ 44.4**	1.34*/ 1.78**	-4 @ 22Gb/s	80	0.25 x 0.39	90nm CMOS
[5] VLSI'12	25	59*	2.36*	—	—	3.6 x 5.3***	65nm CMOS

*TIA/LA only **Total power including output buffer ***Four channels ^Electrical ^^Optical

- Same input sensitivity for both RXs with same TIA but shared-inductor RX has better energy efficiency and smaller chip sizes

Conclusion

- Two 25-28Gb/s optical RXs in 28nm HPM CMOS
  - Same TIA/Offset/LPF/Buffer for both RXs; only LA differs
  - Conventional 25Gb/s RX occupies 0.89 x 0.81 mm^2
  - Shared-inductor 28Gb/s RX occupies 0.6 x 0.53 mm^2
    - 60% area reduction excluding buffer; 56% reduction including buffer
- State-of-the-art energy efficiency for 25-28Gb/s RX
  - 1.55pJ/bit at 25Gb/s for conventional-peaking RX
  - 1.03pJ/bit at 28Gb/s for shared-inductor RX
- Shared-inductor peaking is a good candidate for the next-generation optical and electrical link transceivers
  - Shorter signal routing and smaller layout paracitics
  - Suitable for cost-effective high-speed transceivers

A Sub-1.75W Full-Duplex 10GBASE-T Transceiver in 40nm CMOS

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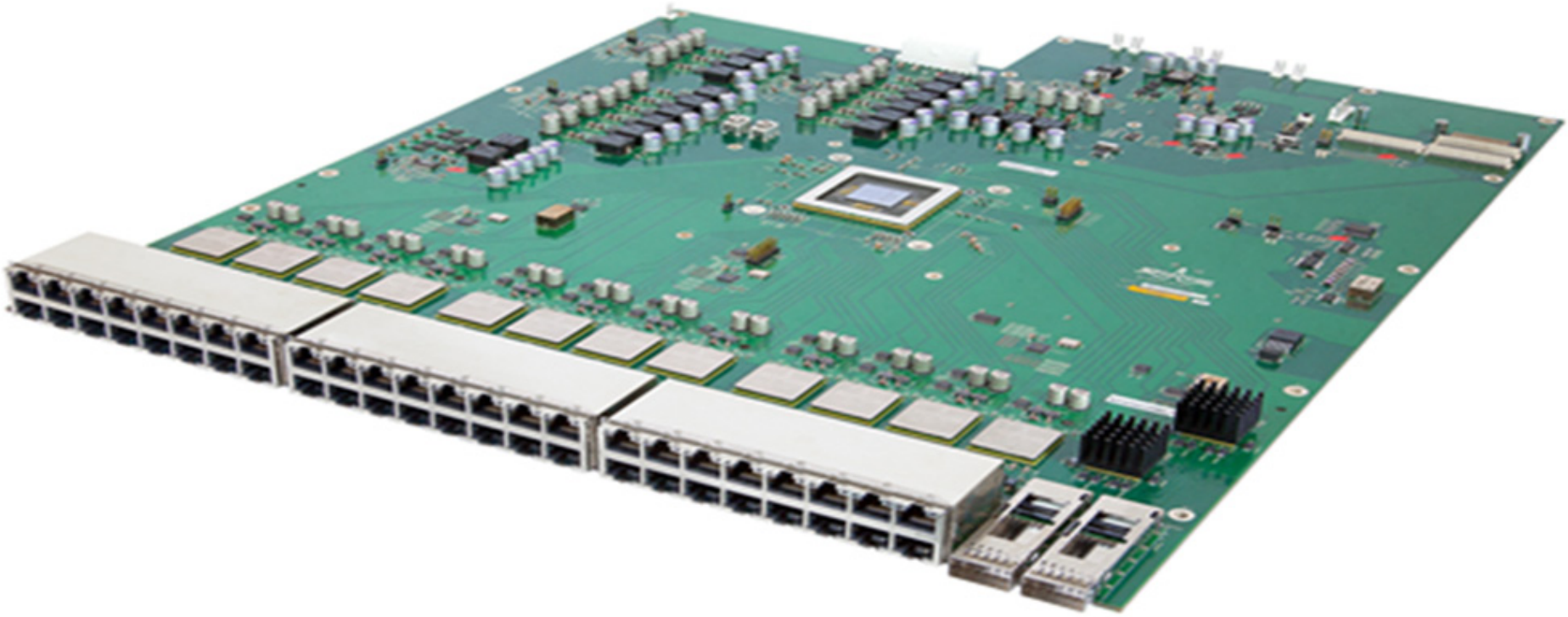
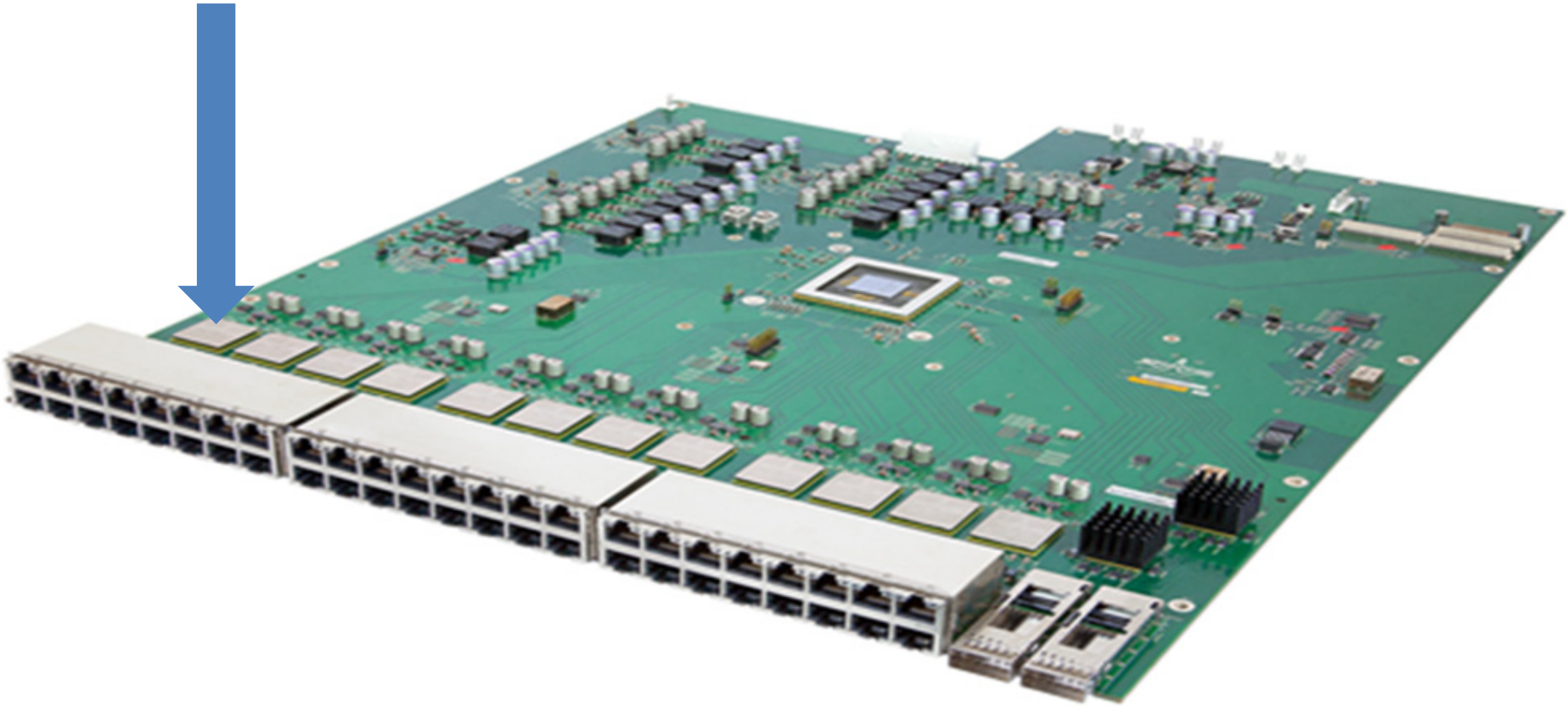
Broadcom Netherlands B.V., Bunnik, The Netherlands

The Environment

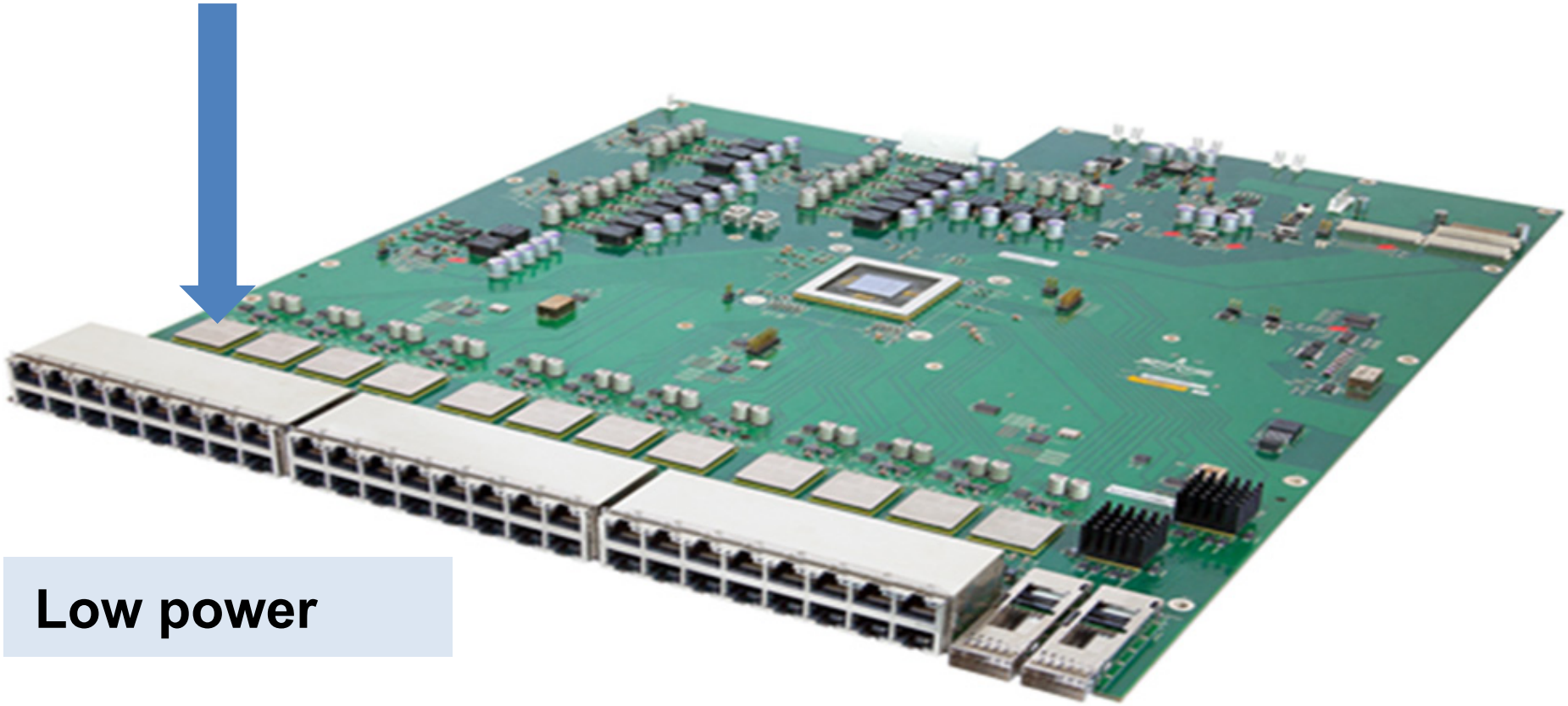
48-port 10GBASE-T Ethernet Switch



48-port 10GBASE-T Ethernet Switch

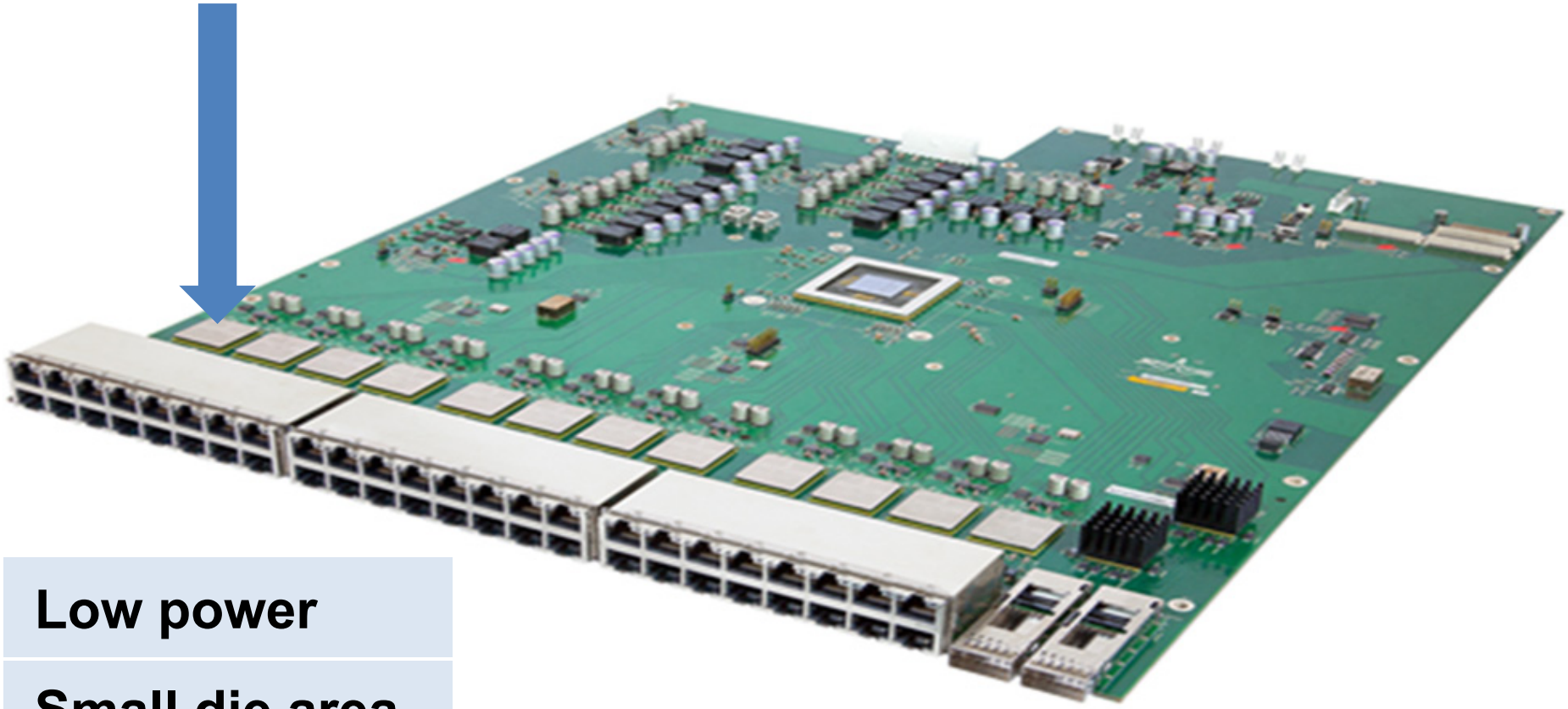


48-port 10GBASE-T Ethernet Switch



Low power

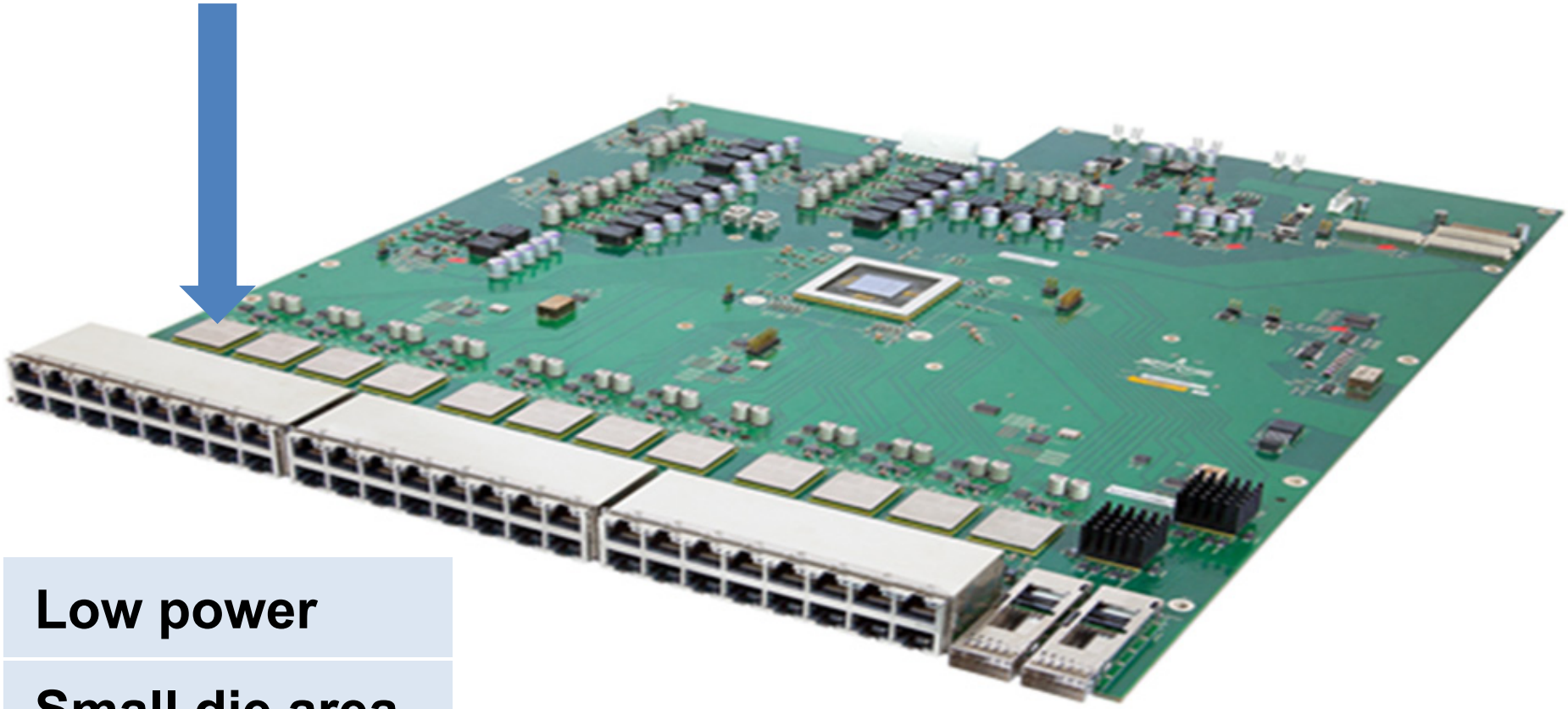
48-port 10GBASE-T Ethernet Switch



Low power

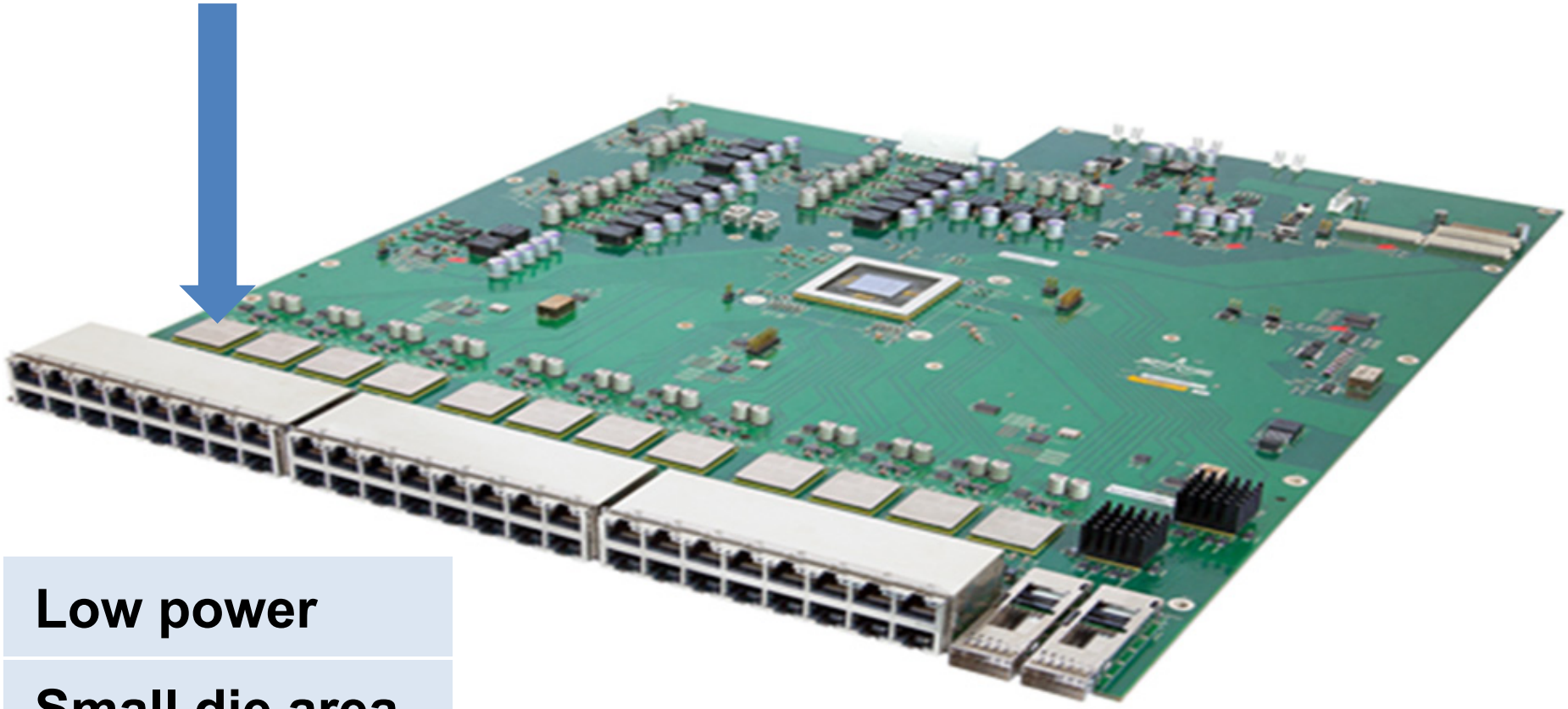
Small die area

48-port 10GBASE-T Ethernet Switch



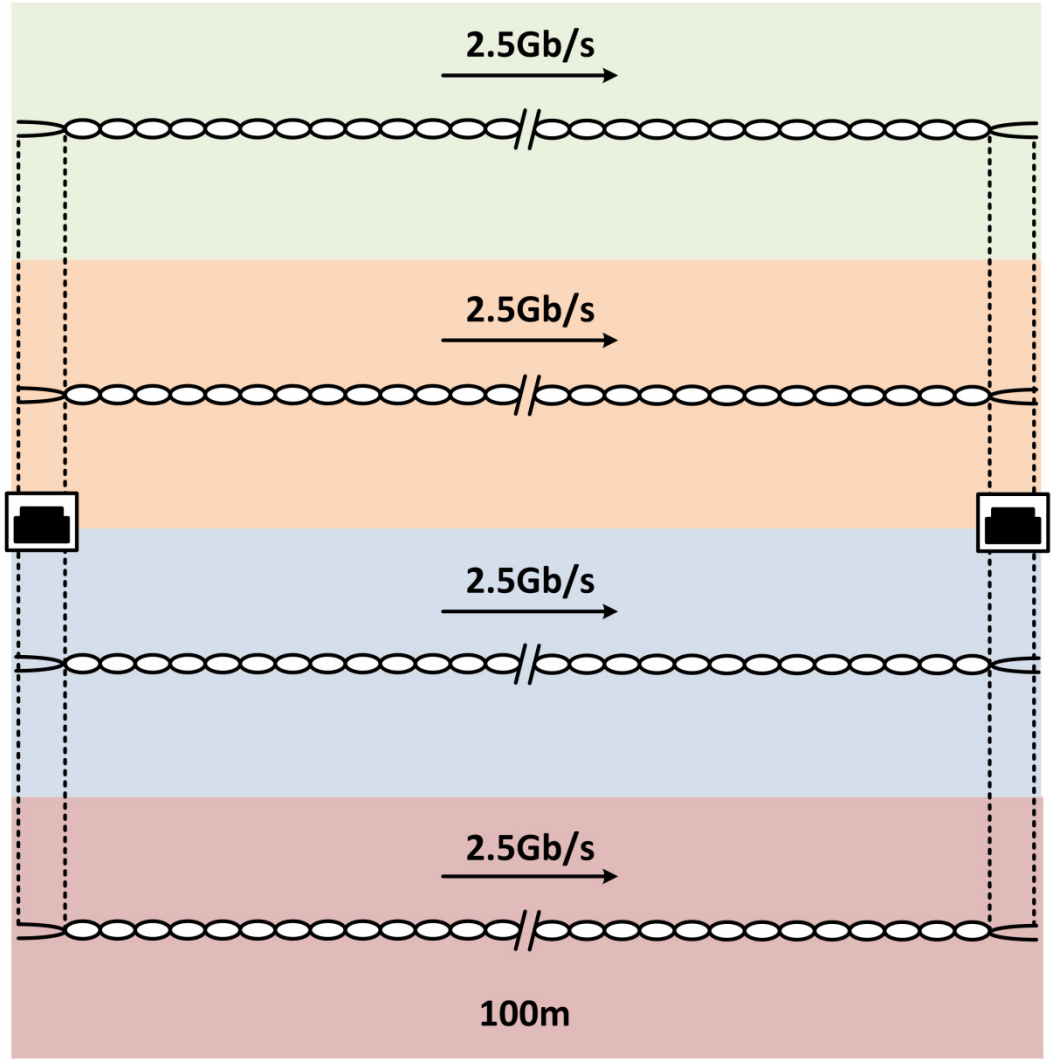
- **Low power**
- **Small die area**
- **Low EMI**

48-port 10GBASE-T Ethernet Switch



- Low power
- Small die area
- Low EMI
- Robust

10GBASE-T



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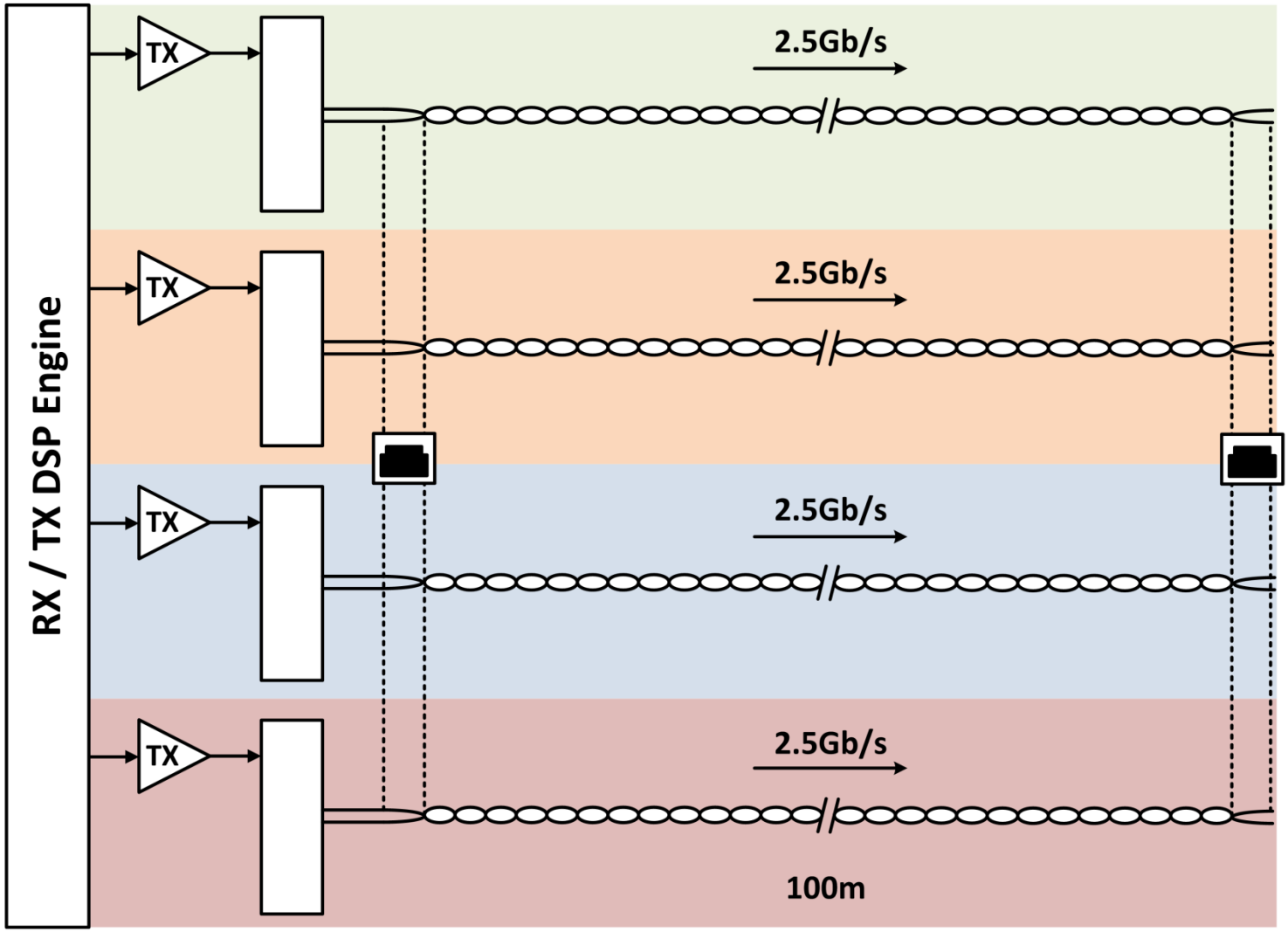

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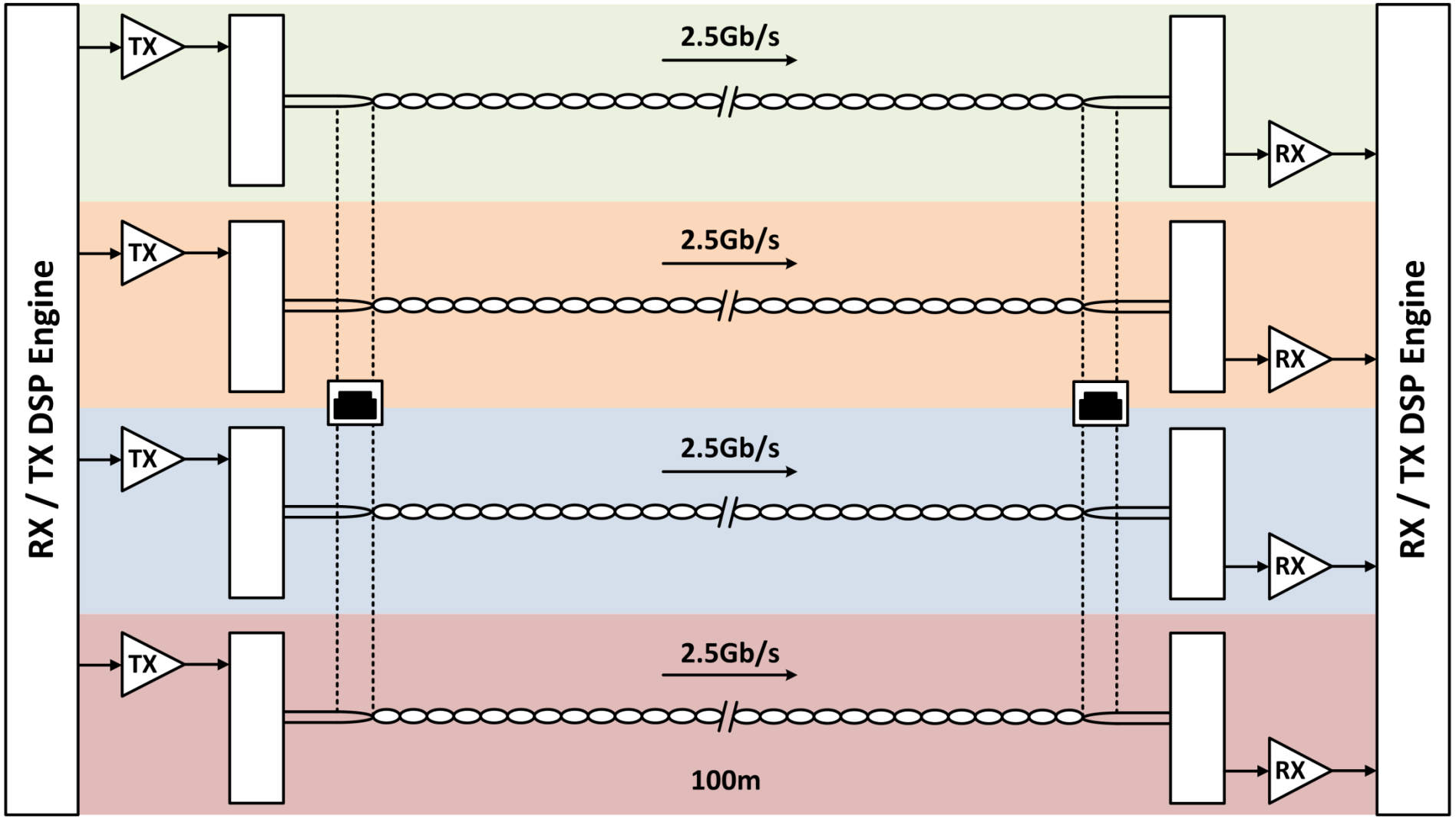

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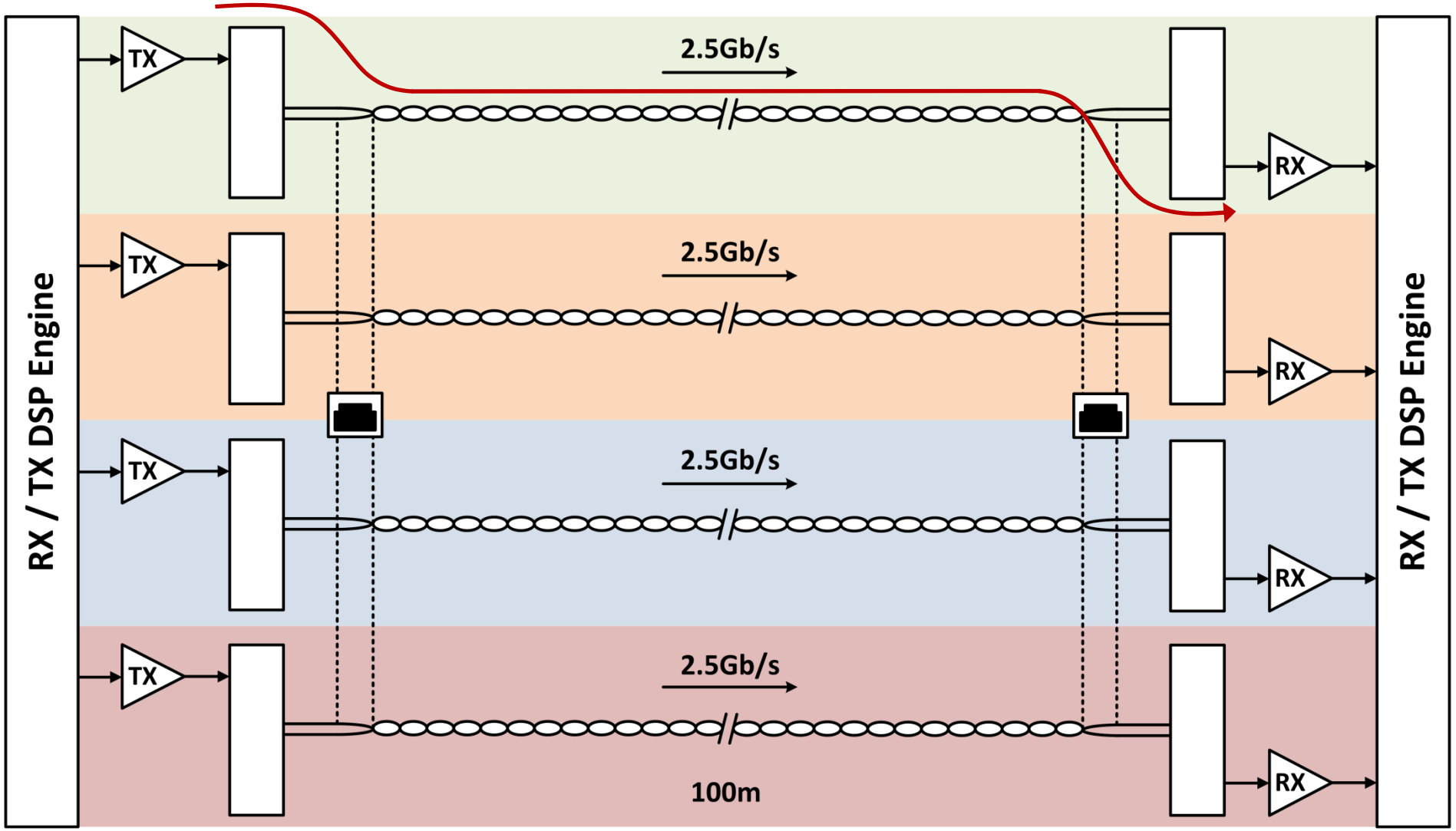

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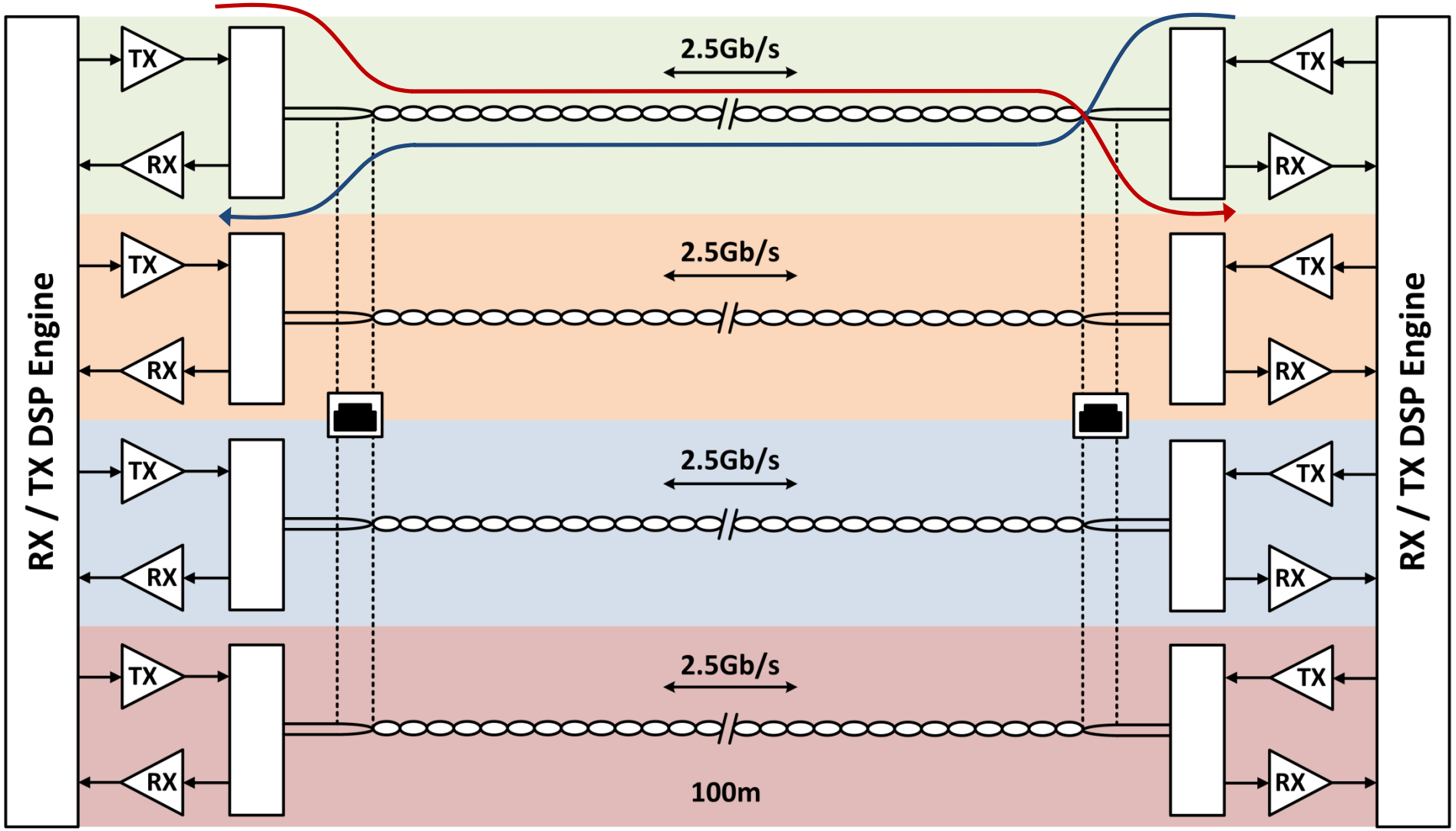

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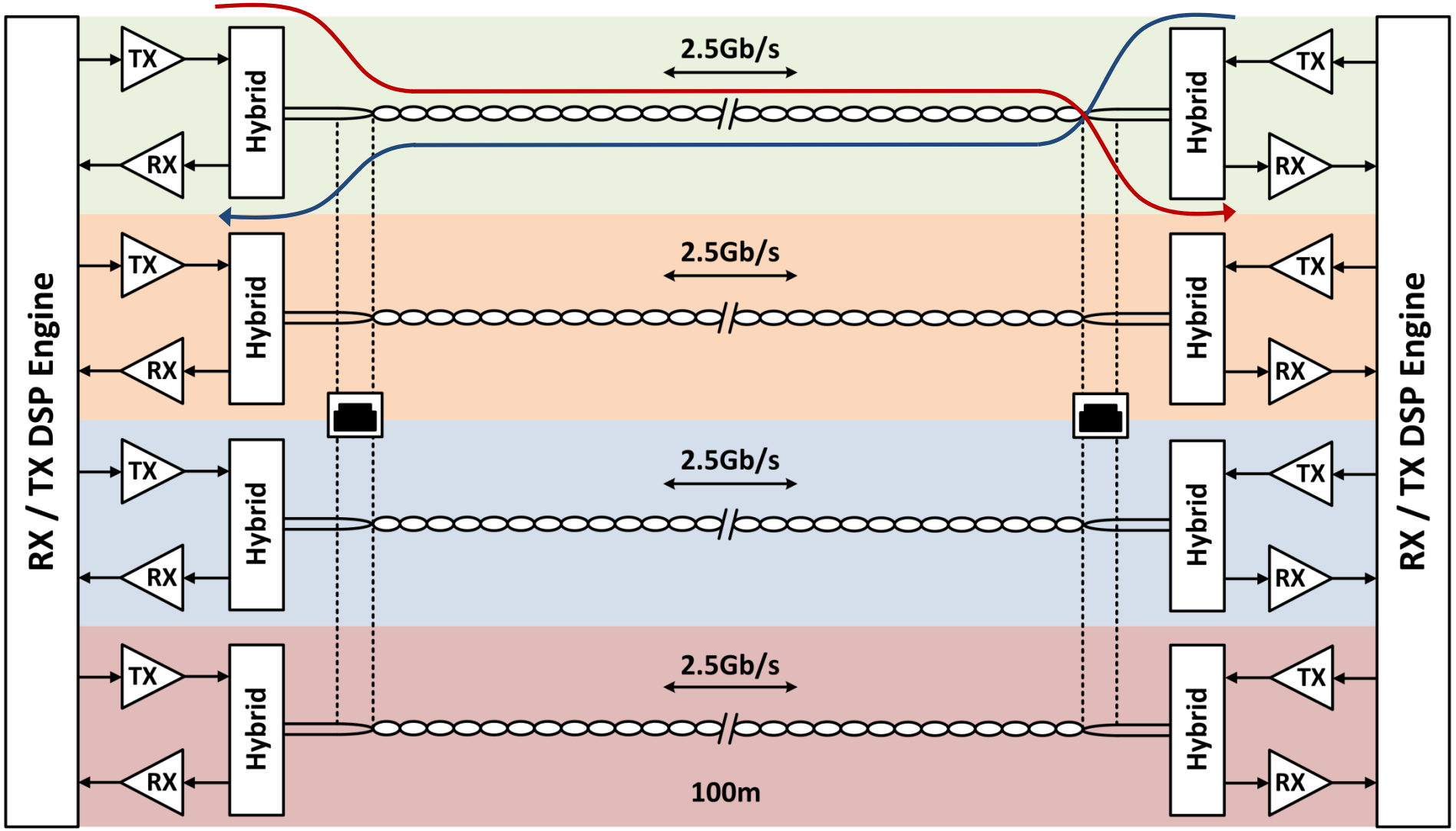

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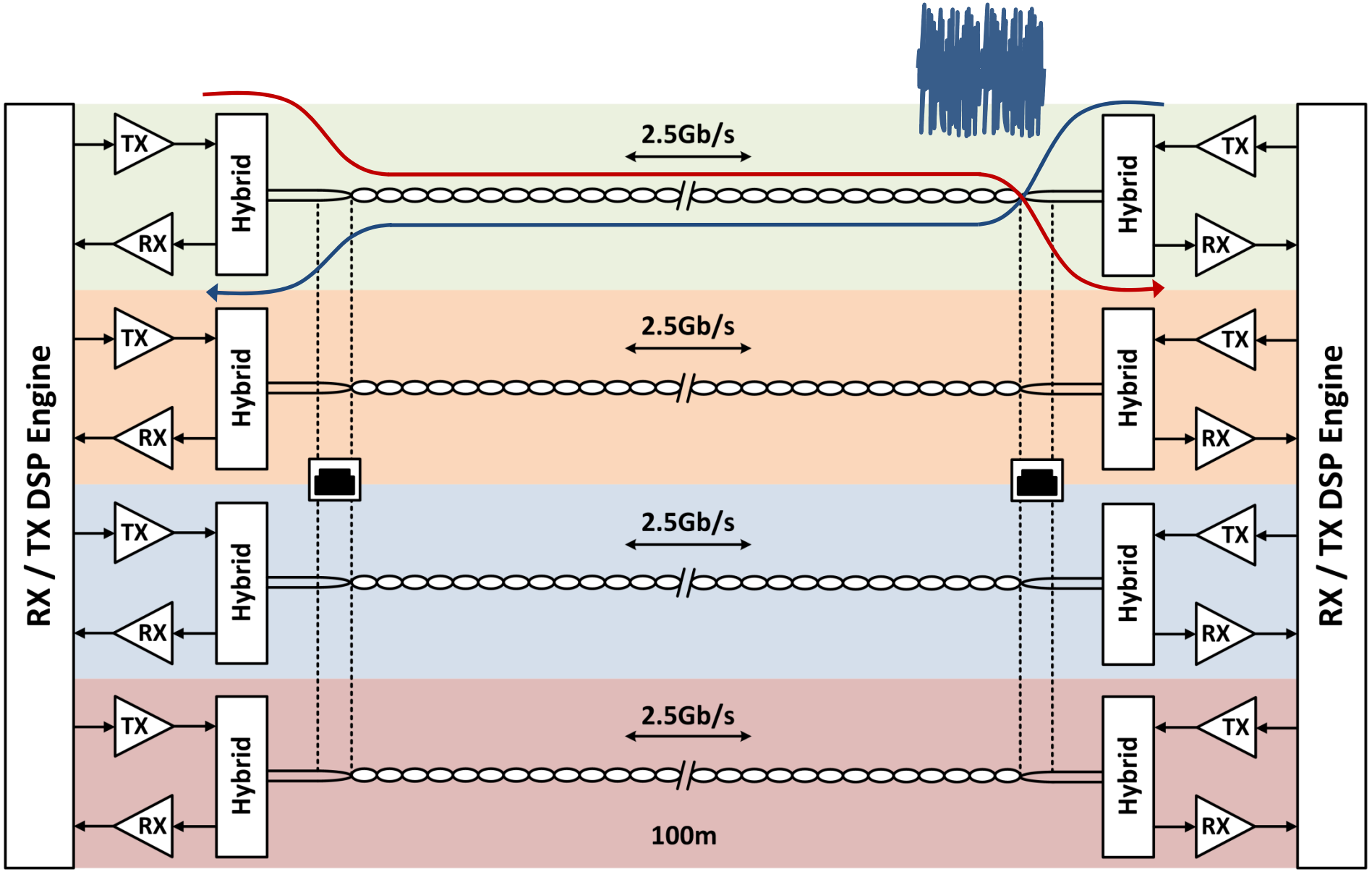

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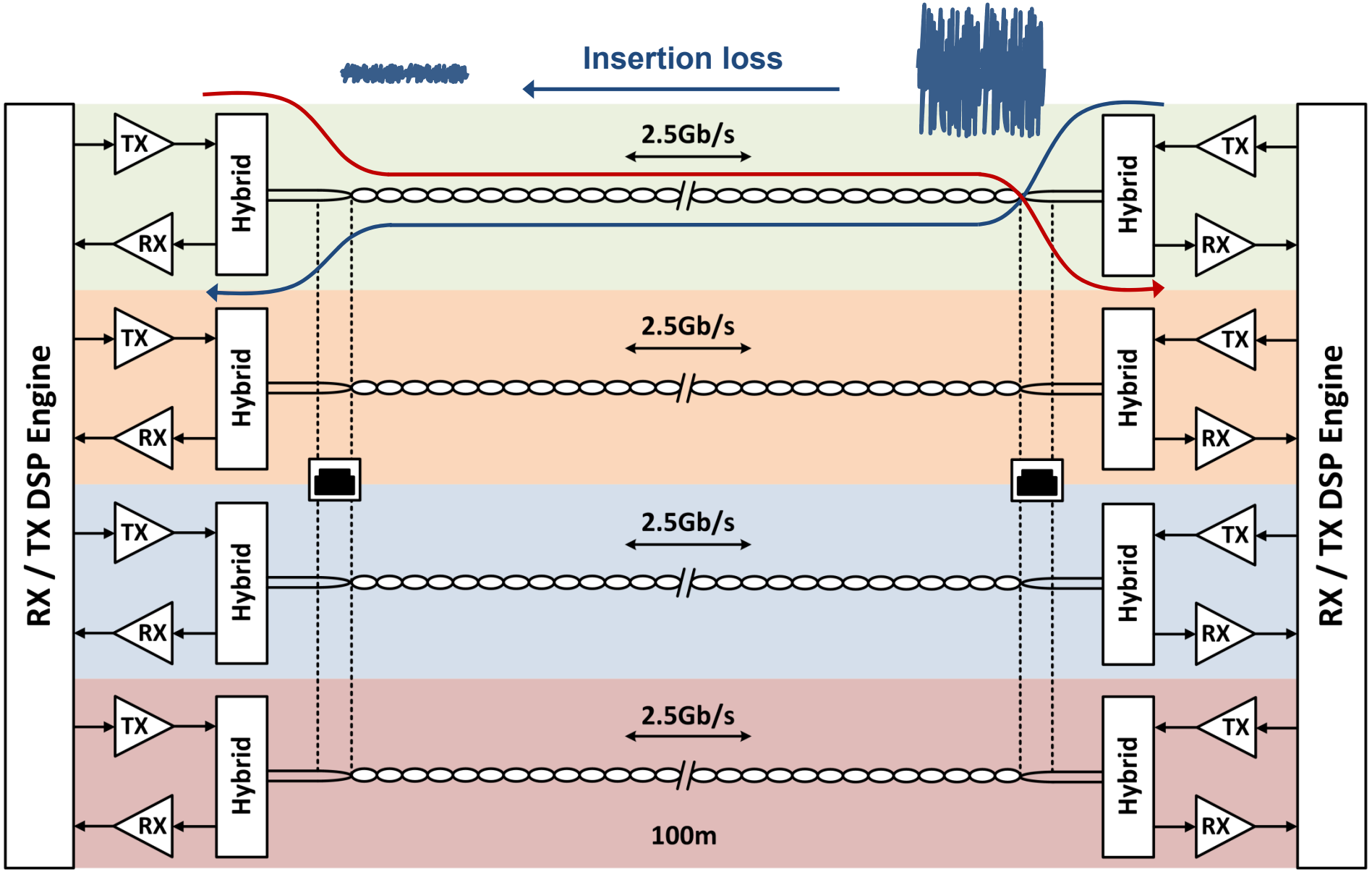

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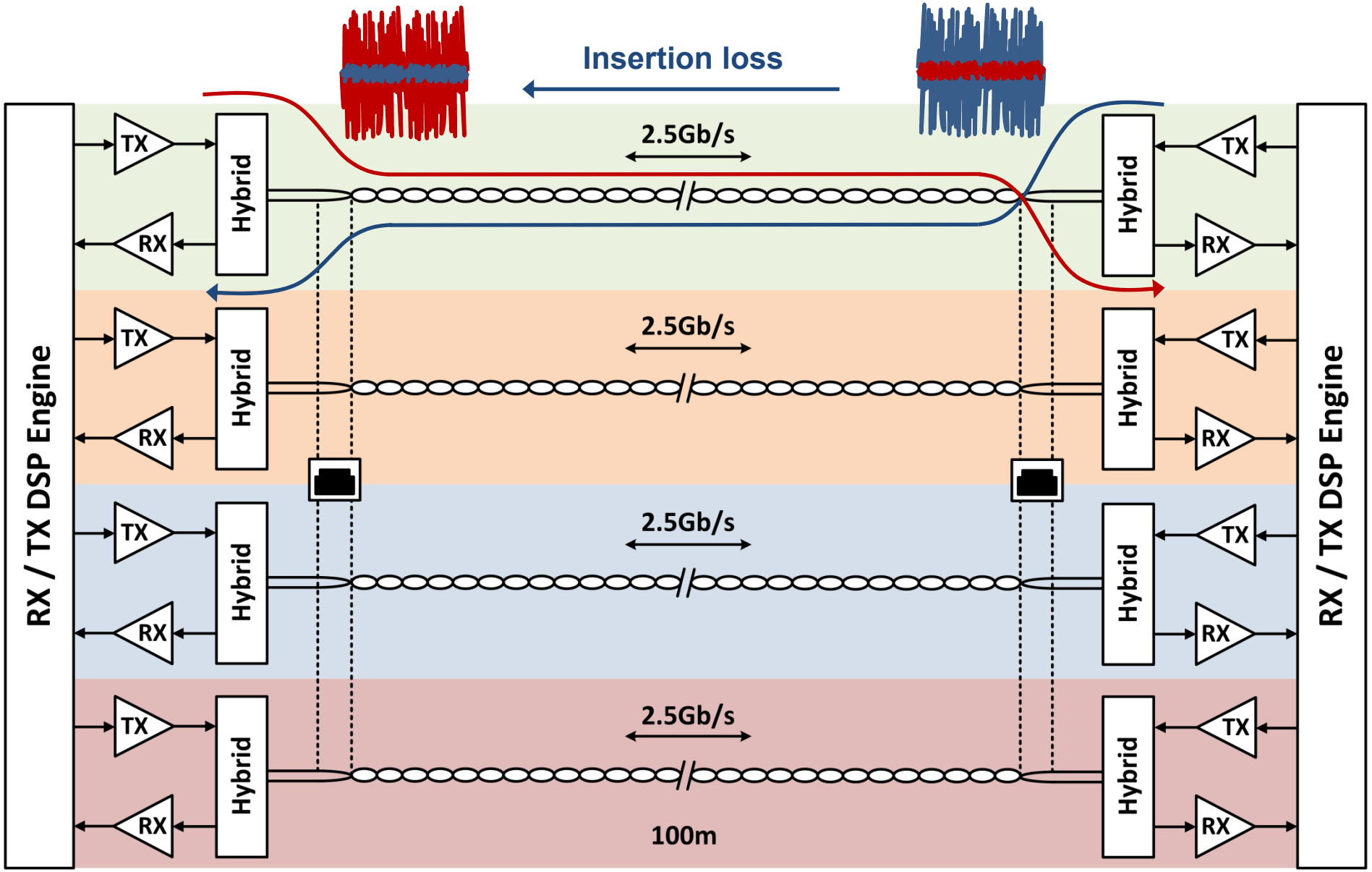
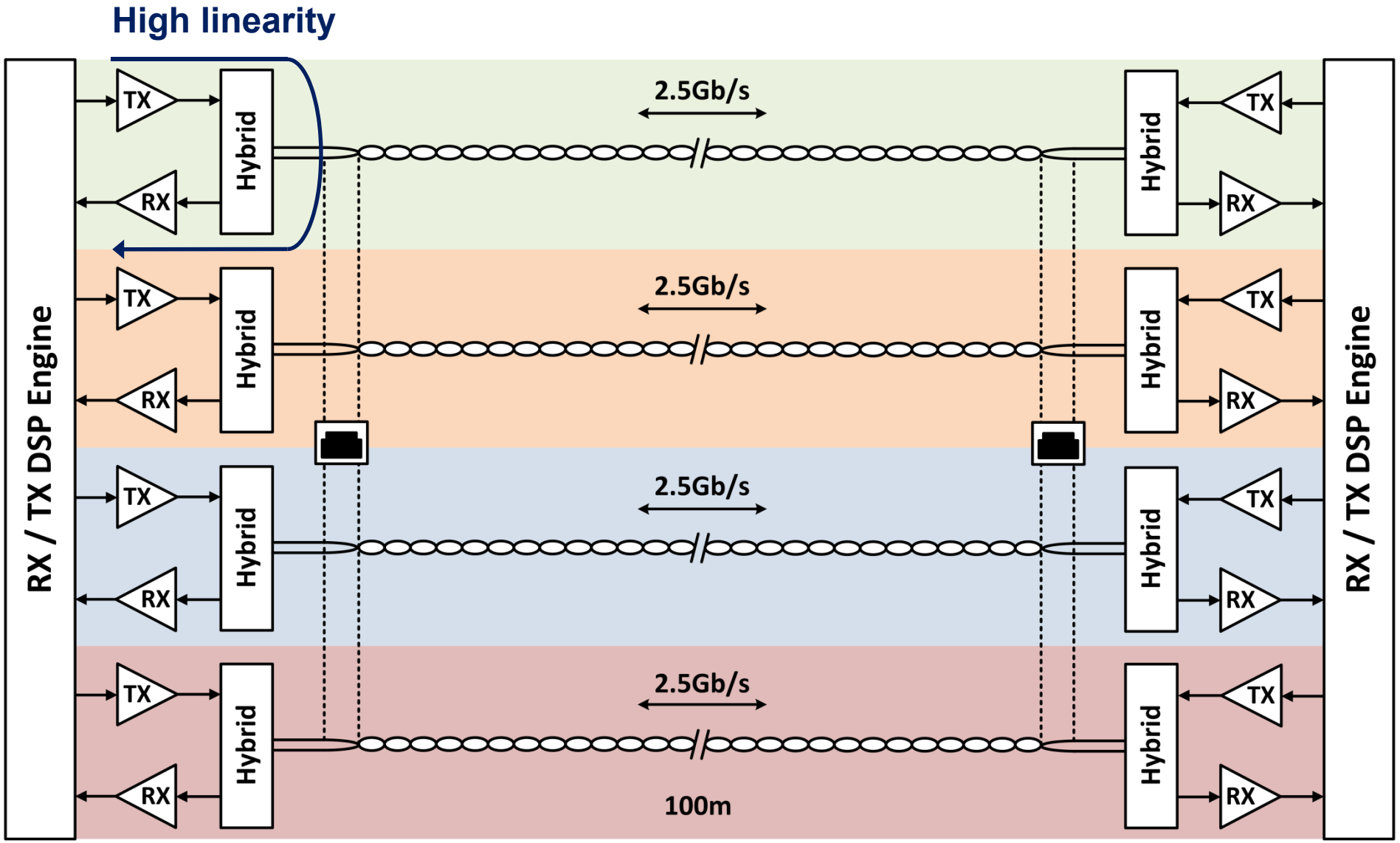
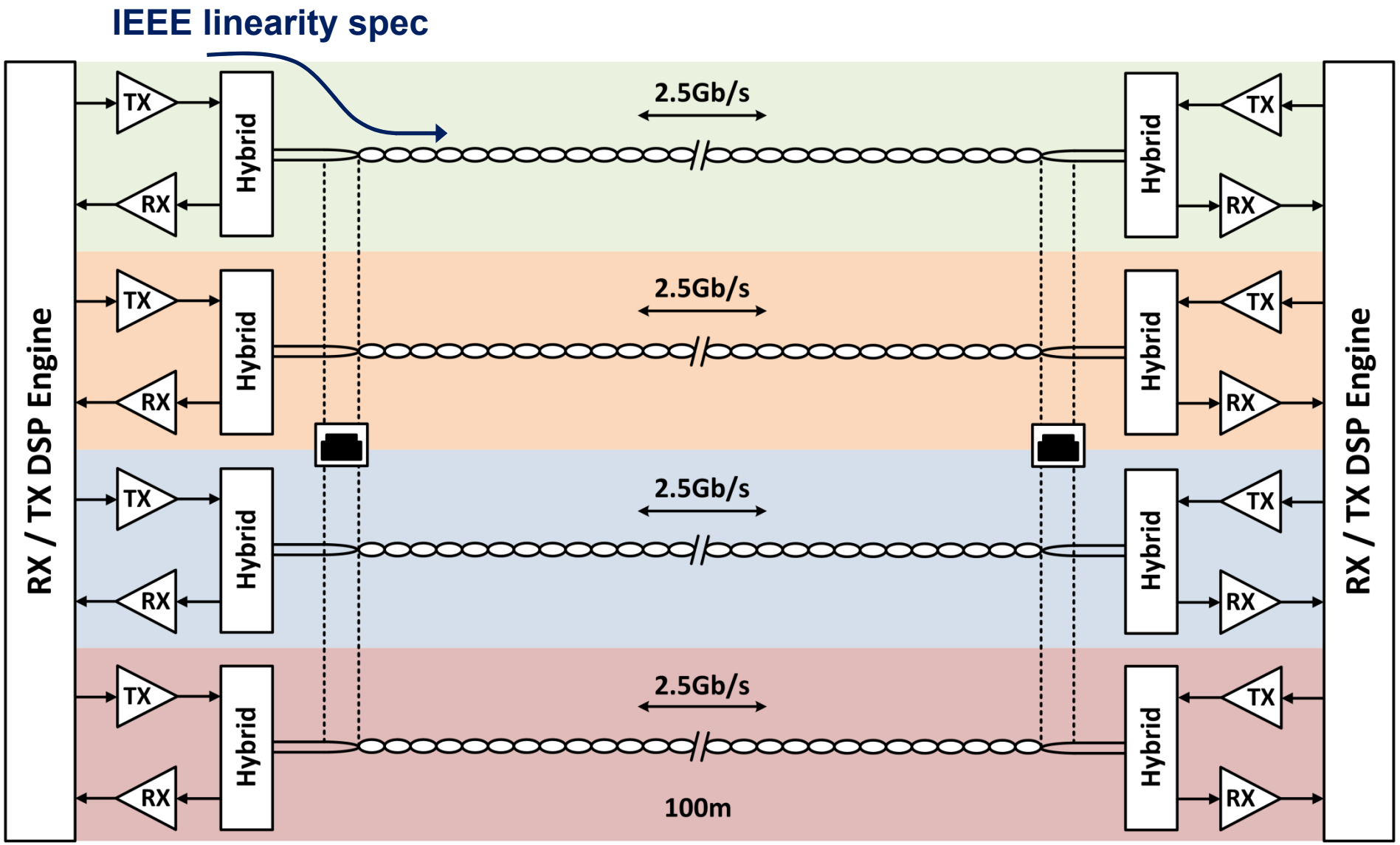


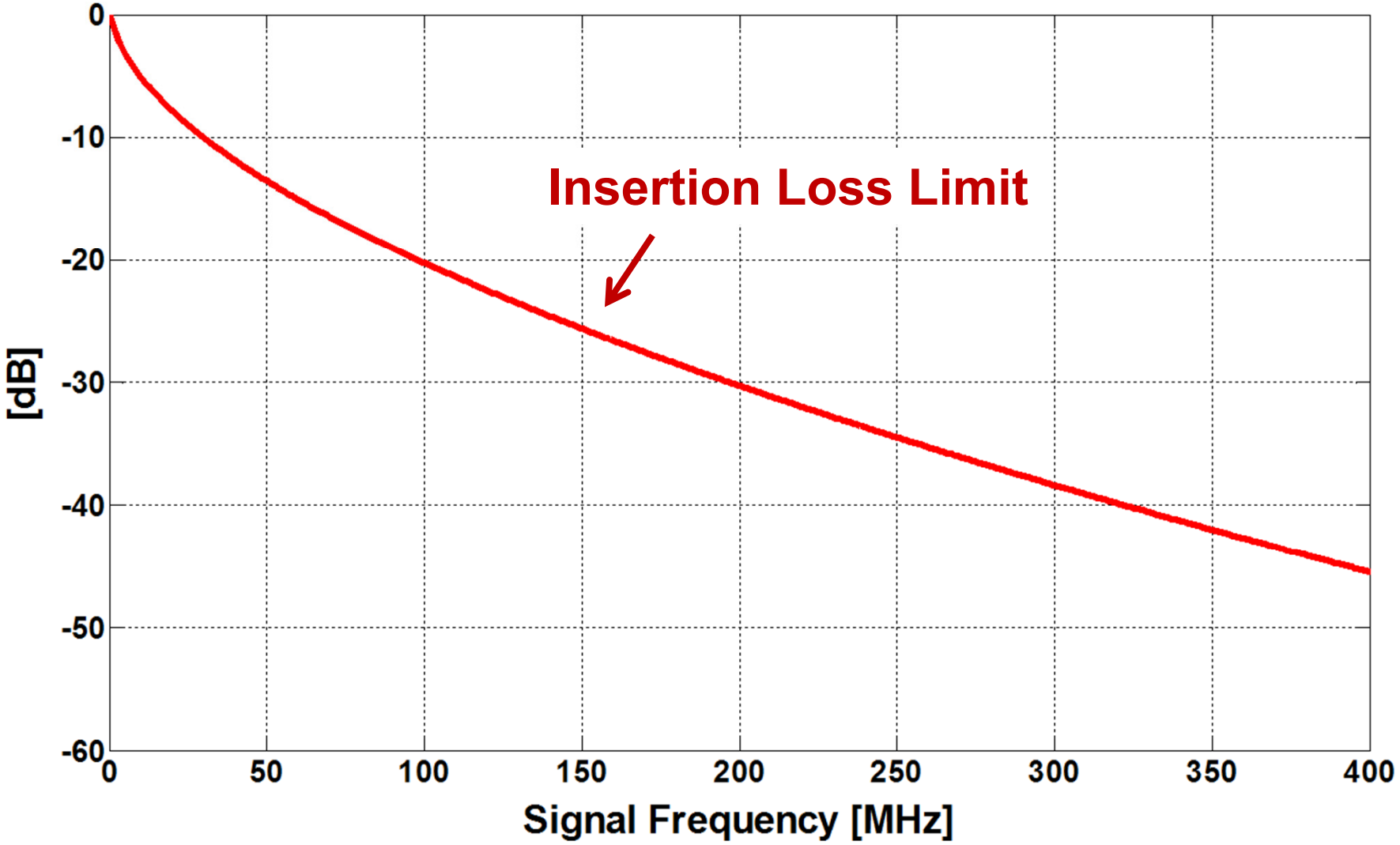
Transceiver Linearity



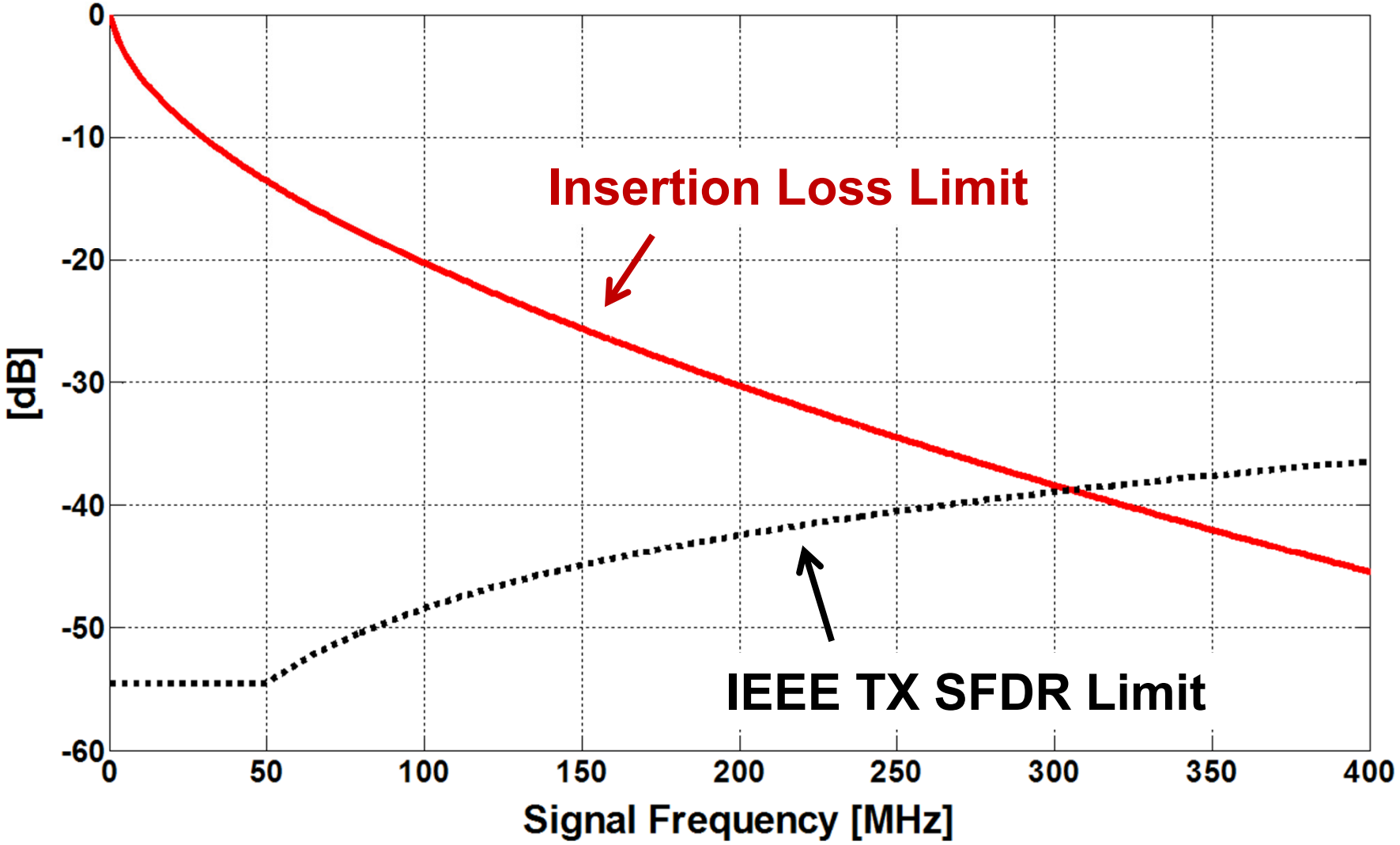
Transceiver Linearity



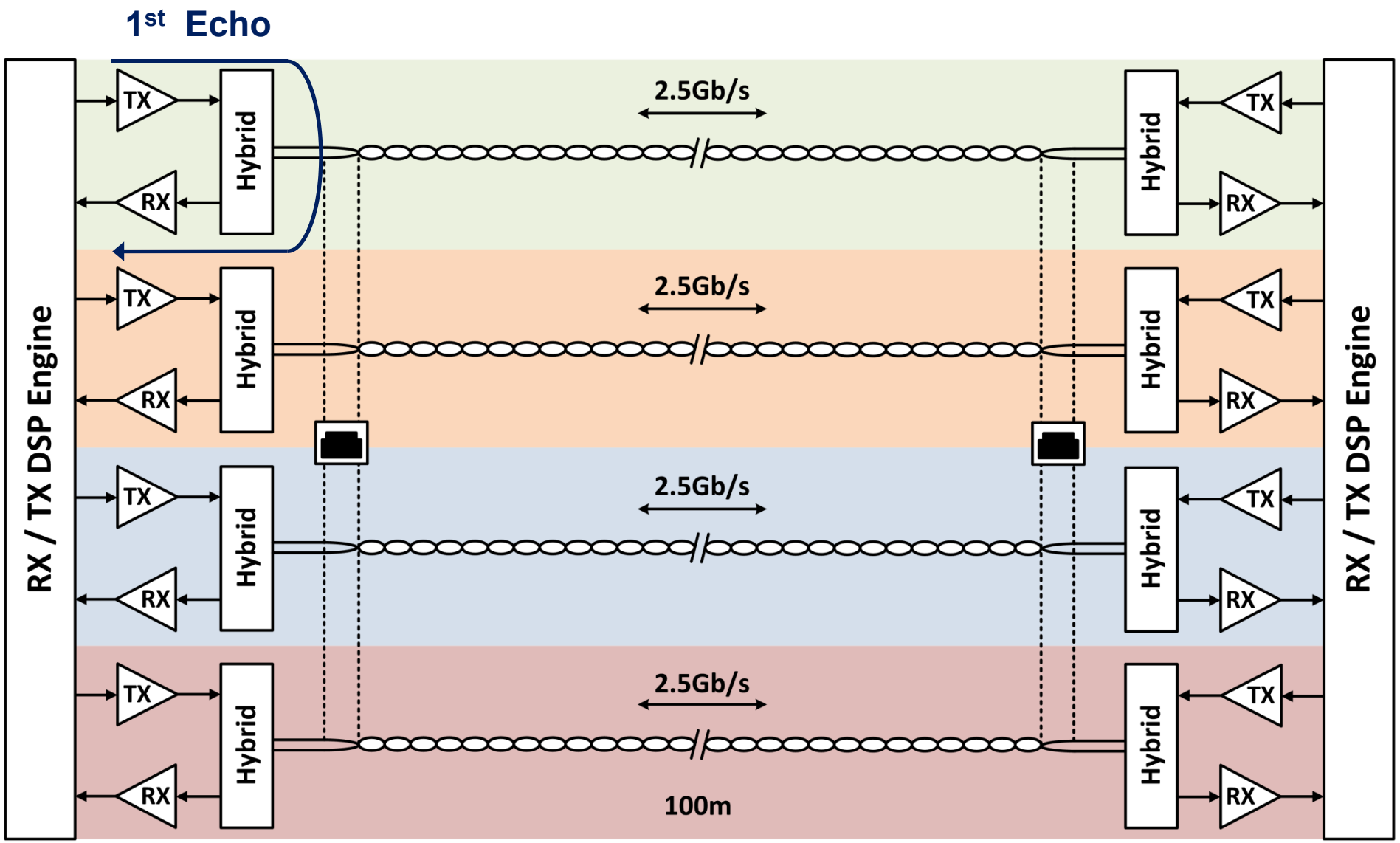
Transceiver Linearity



Transceiver Linearity



Echoes



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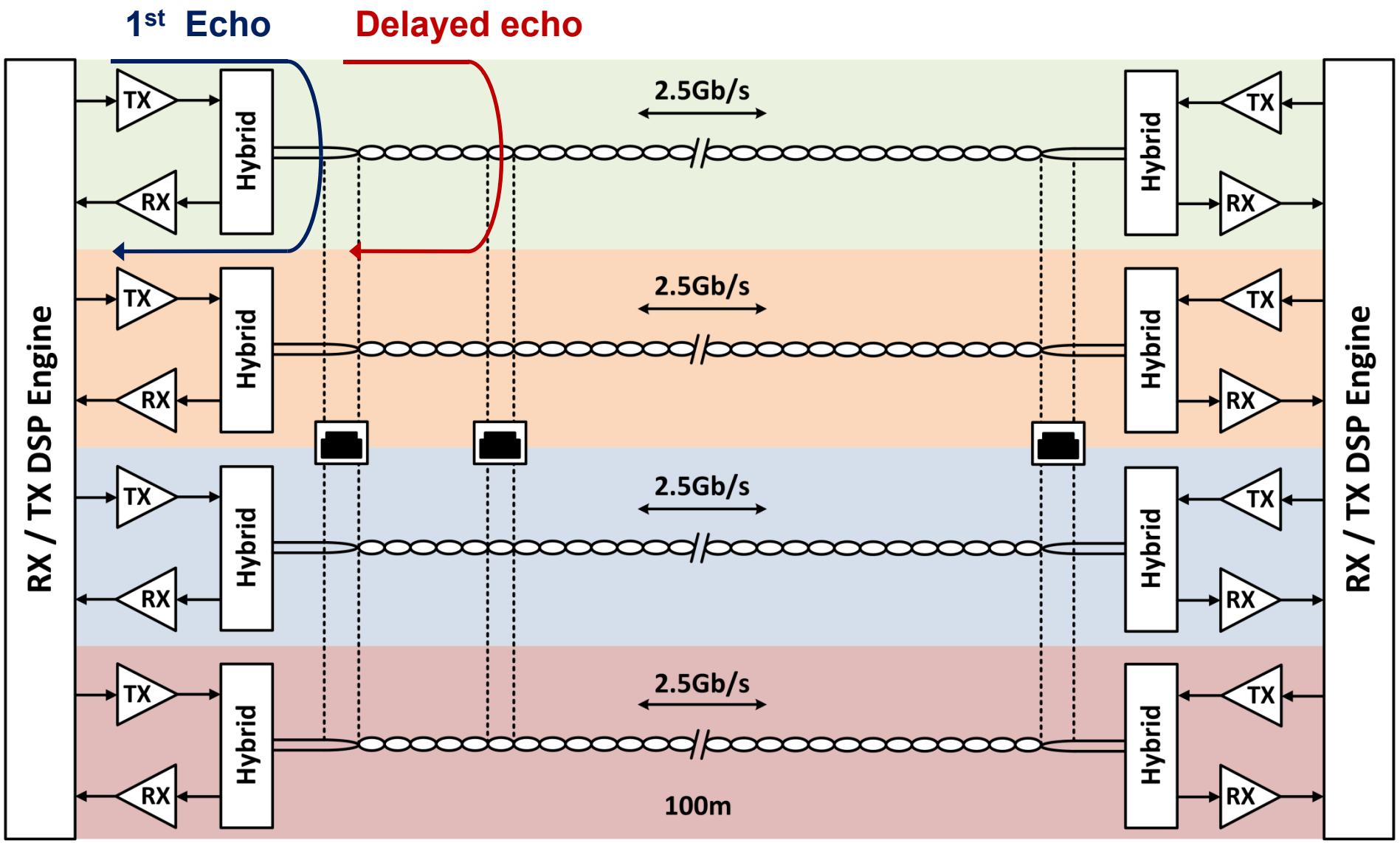
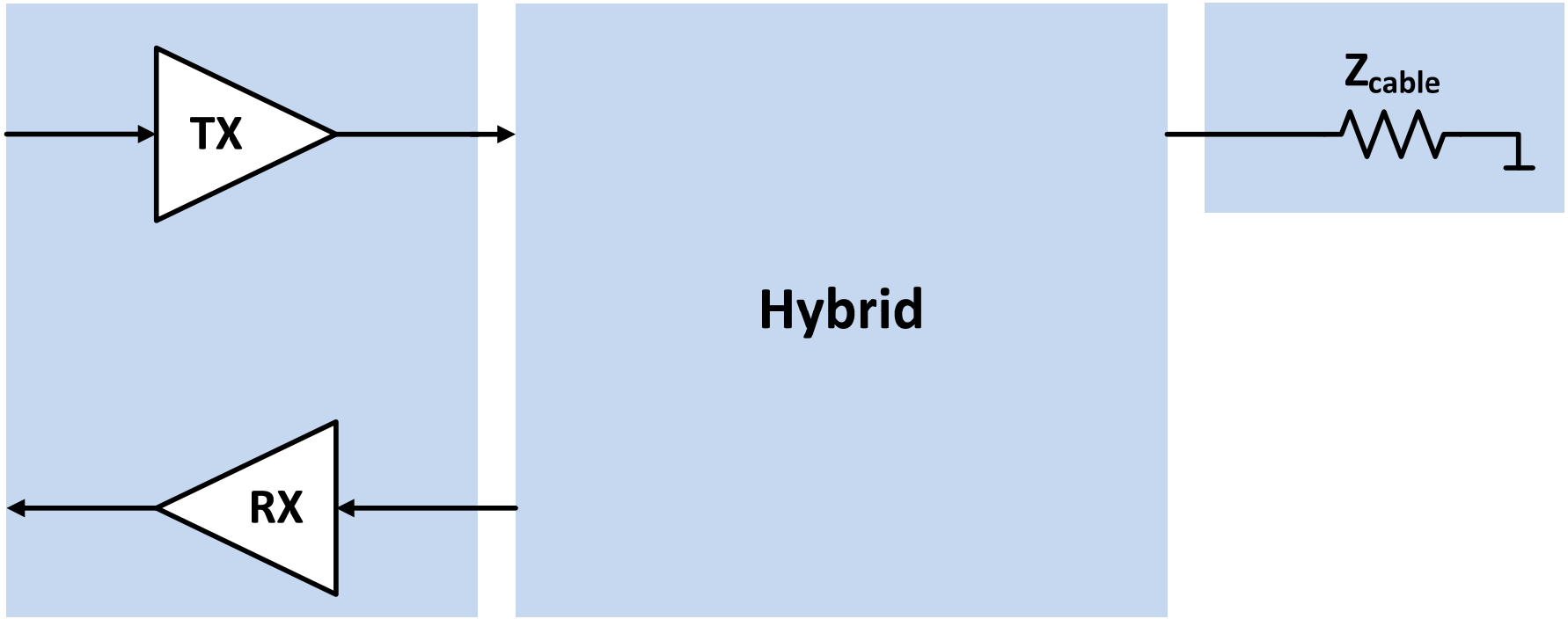
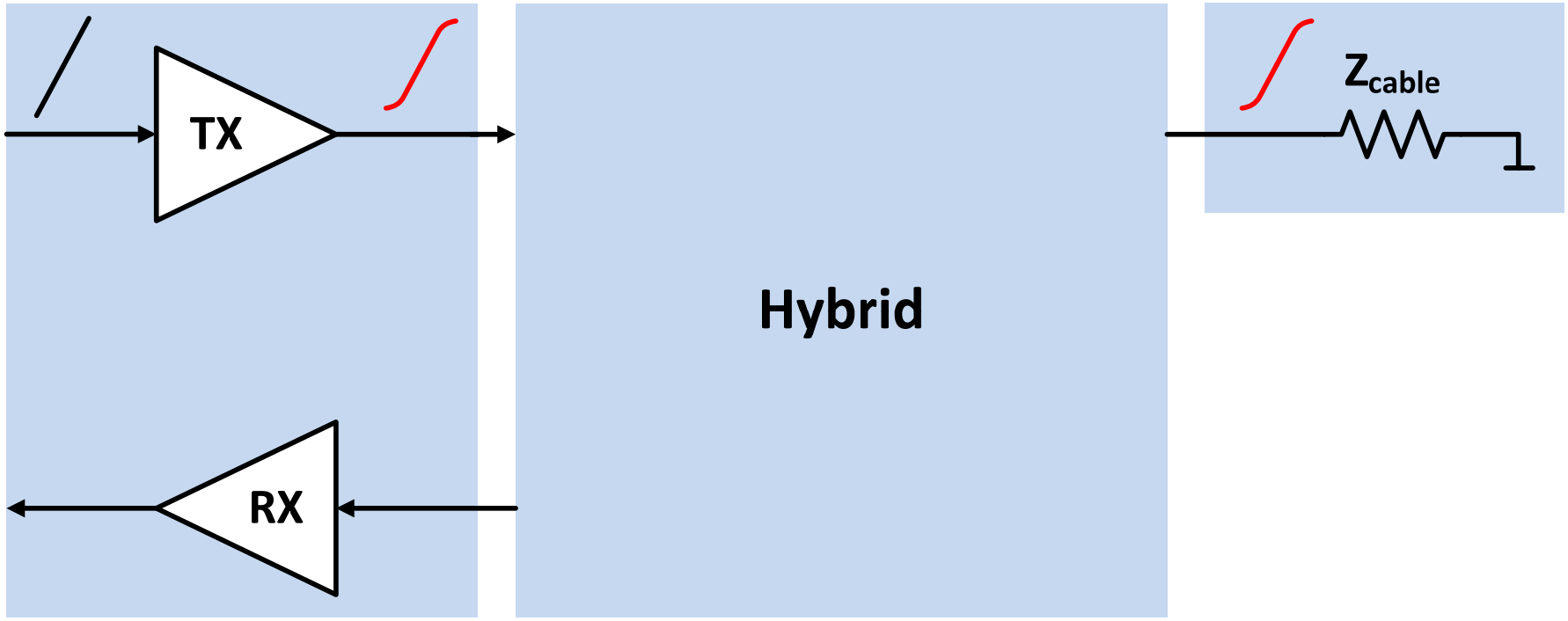


Single DAC Hybrid Architecture



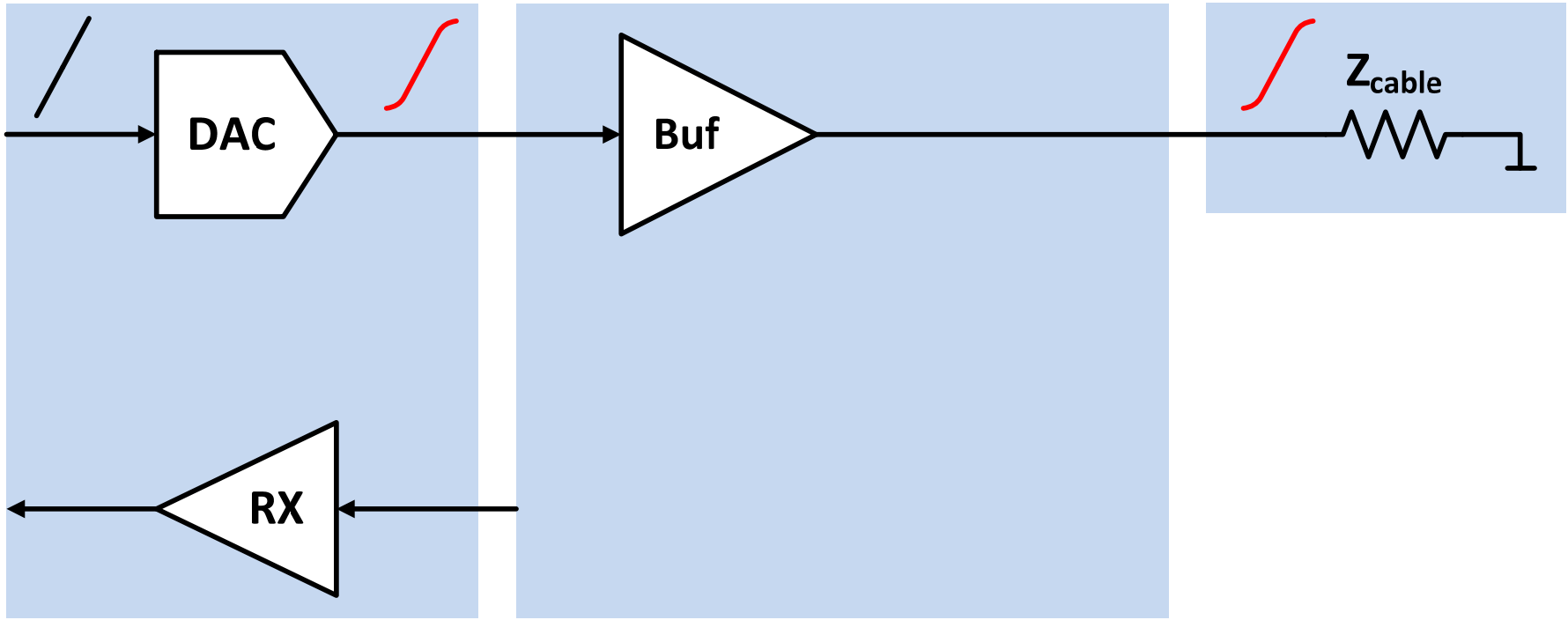
Pros	Cons

Single DAC Hybrid Architecture



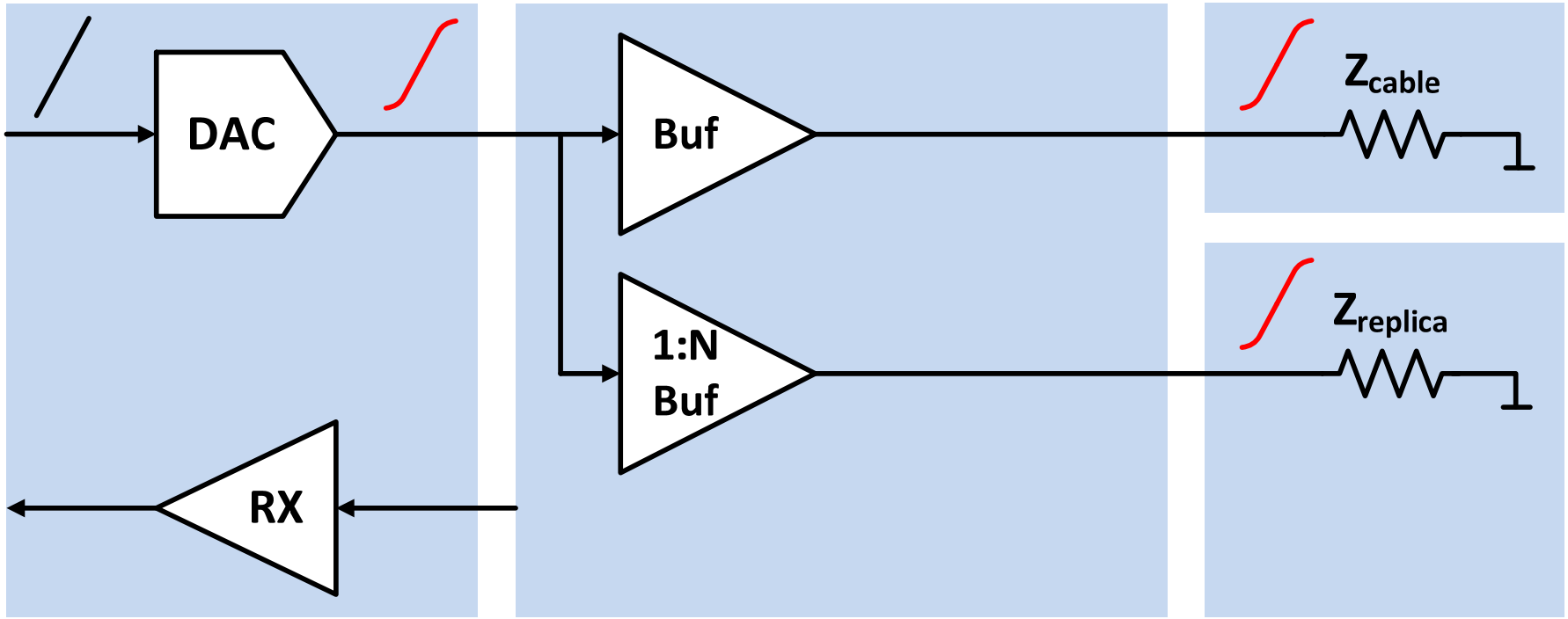
Pros	Cons

Single DAC Hybrid Architecture



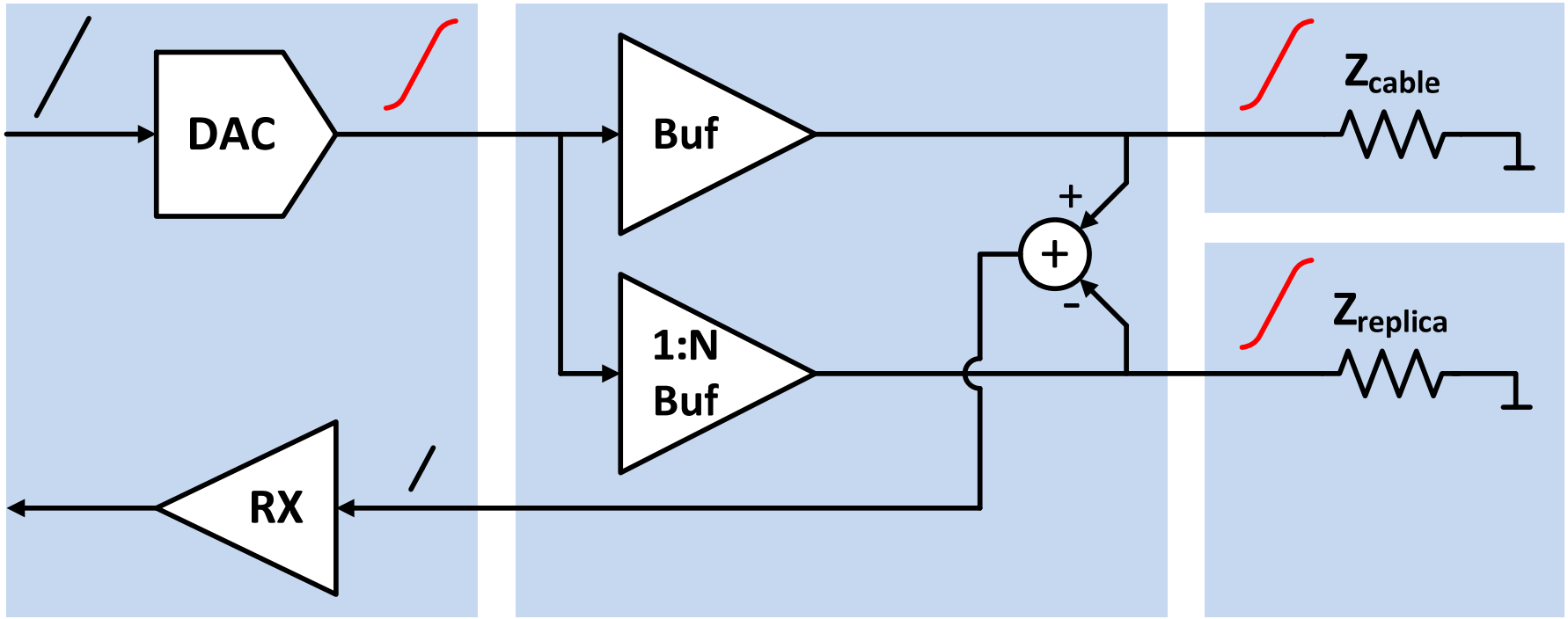
Pros	Cons

Single DAC Hybrid Architecture



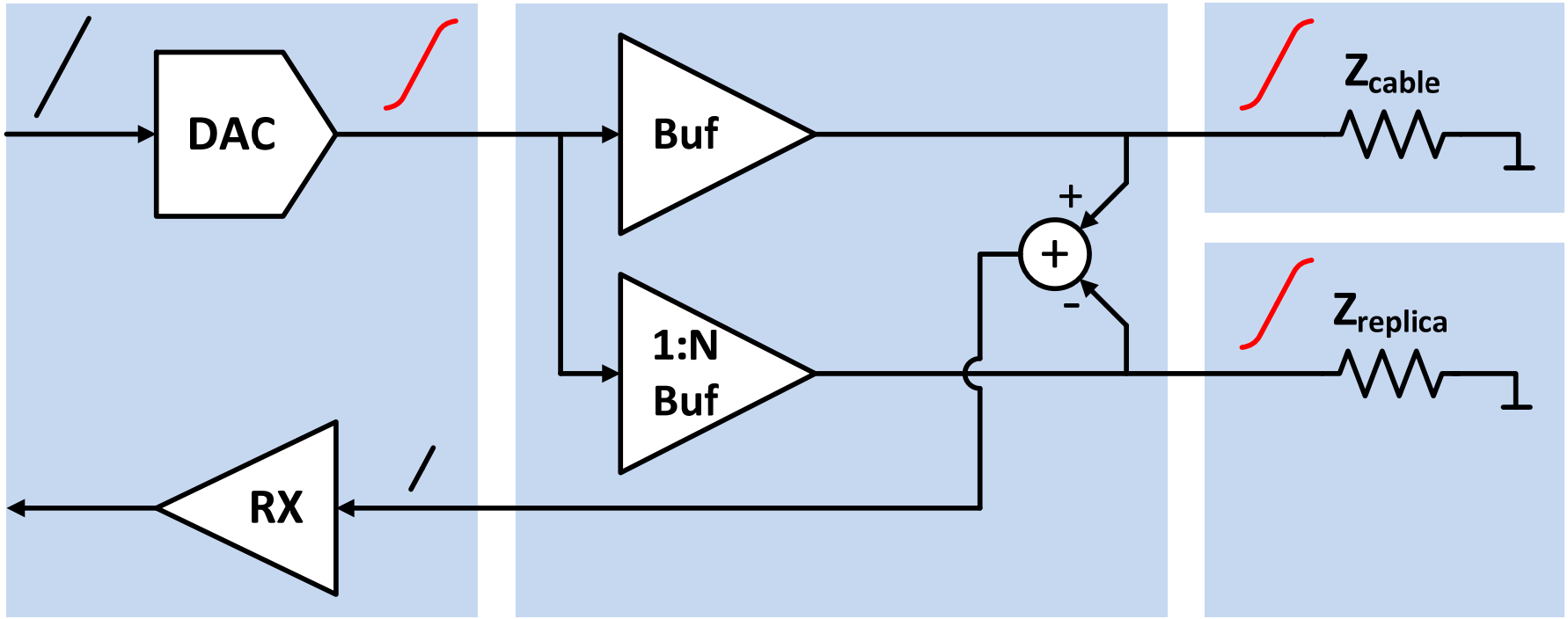
Pros	Cons

Single DAC Hybrid Architecture



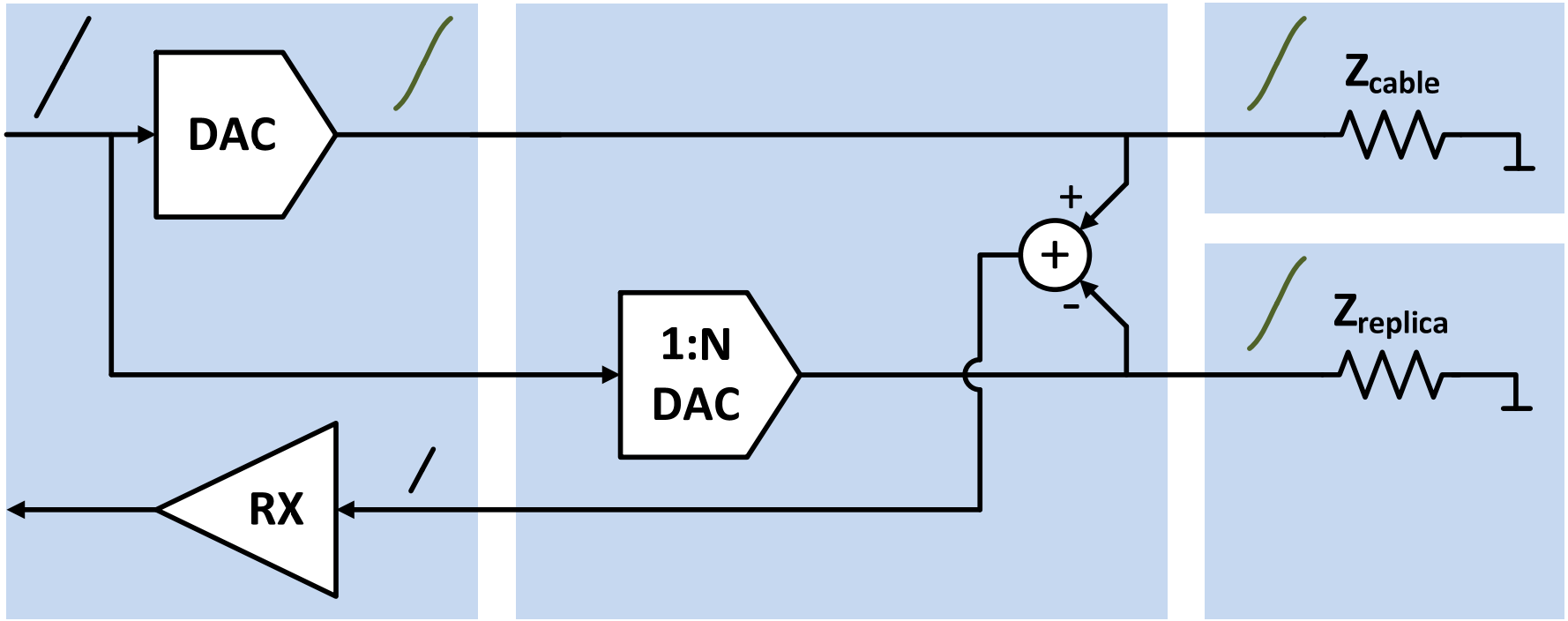
Pros	Cons

Single DAC Hybrid Architecture



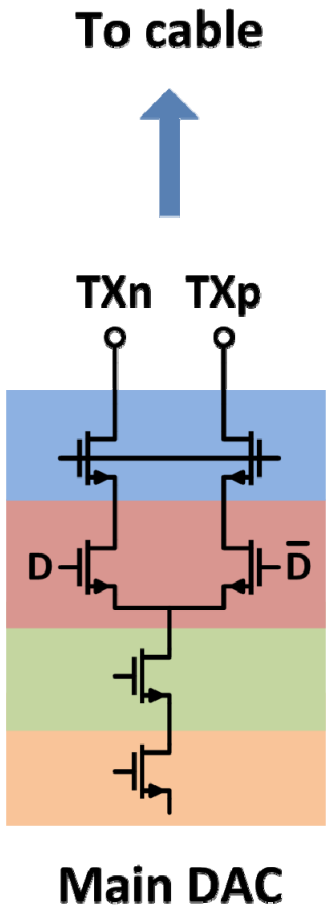
Pros	Cons
No linear DAC required	
	Does rely on NL cancel
	Non-linear delayed echoes
	Not low power / distortion

Double DAC Hybrid Architecture

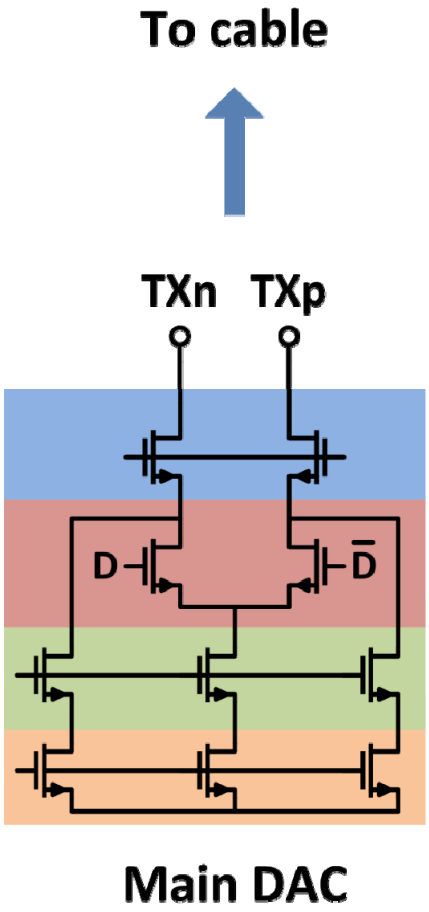


Pros	Cons
	Linear DAC required
Does not rely on NL cancel	
Linear delayed echoes	
Low power	

TX / Hybrid Architecture

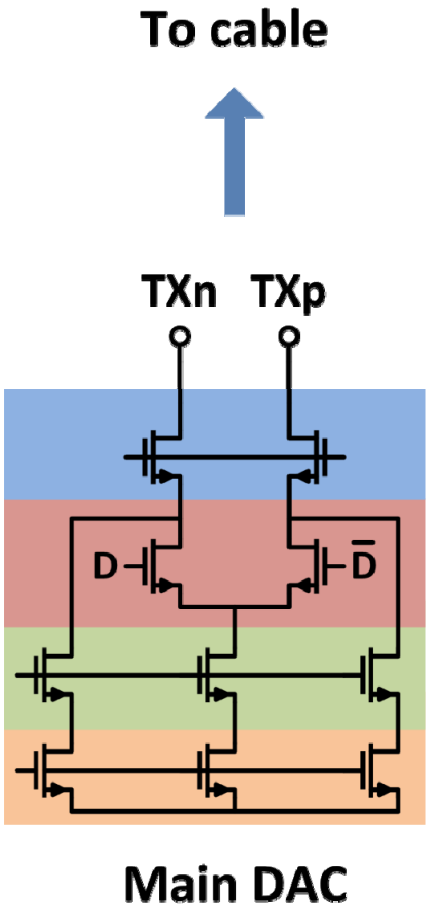


TX / Hybrid Architecture

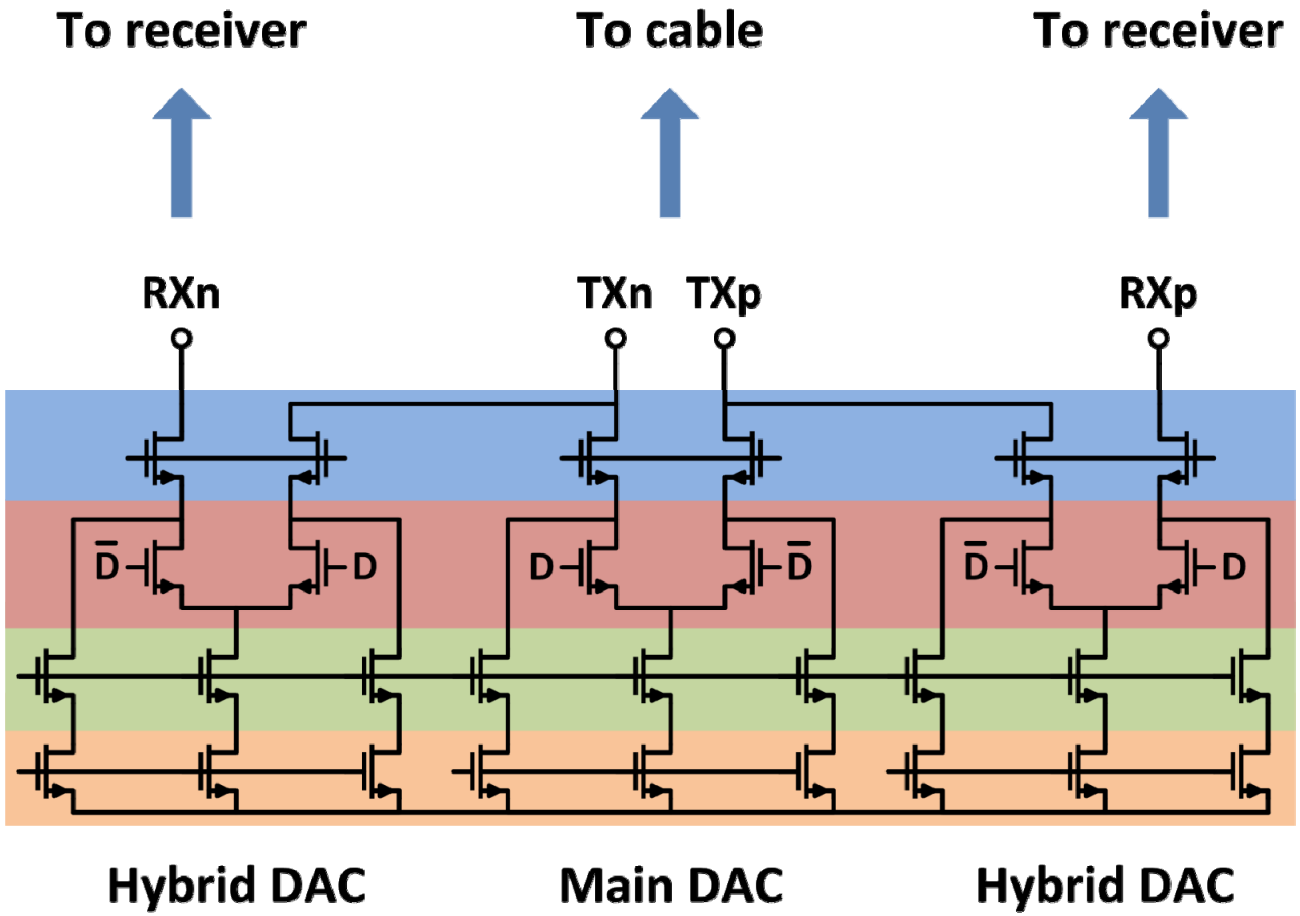


TX / Hybrid Architecture

C.H.Lin et al. ISSCC 2009

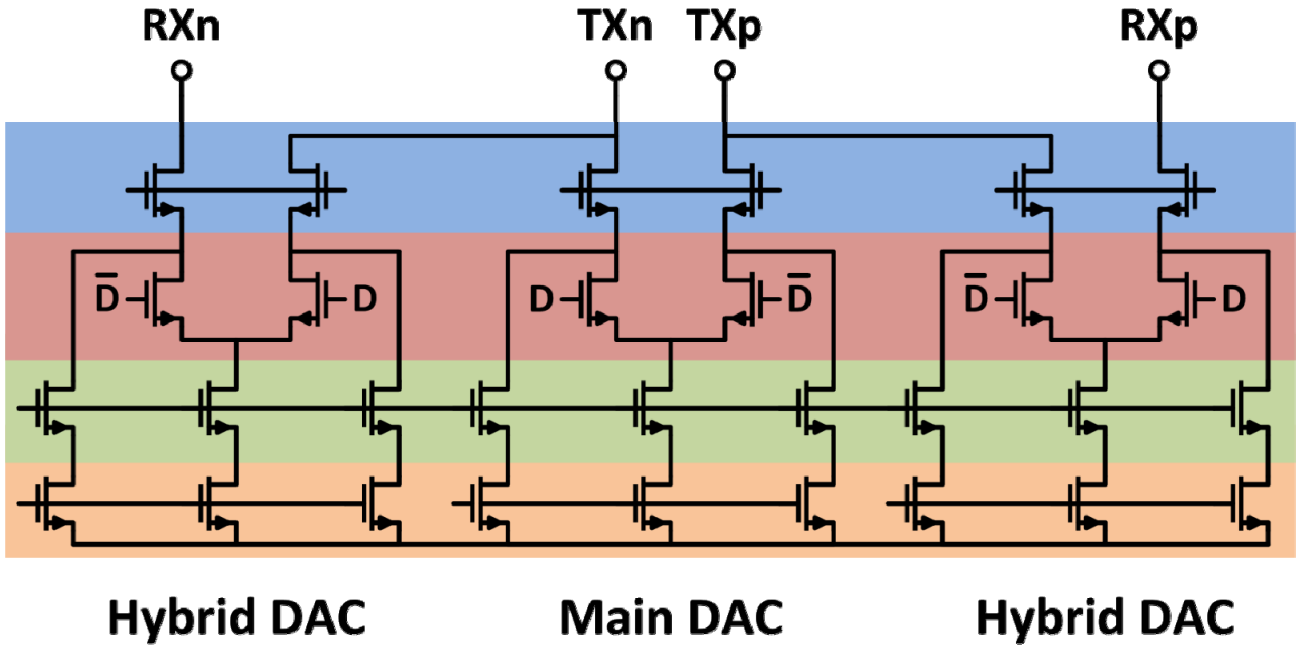


TX / Hybrid Architecture



TX / Hybrid Architecture

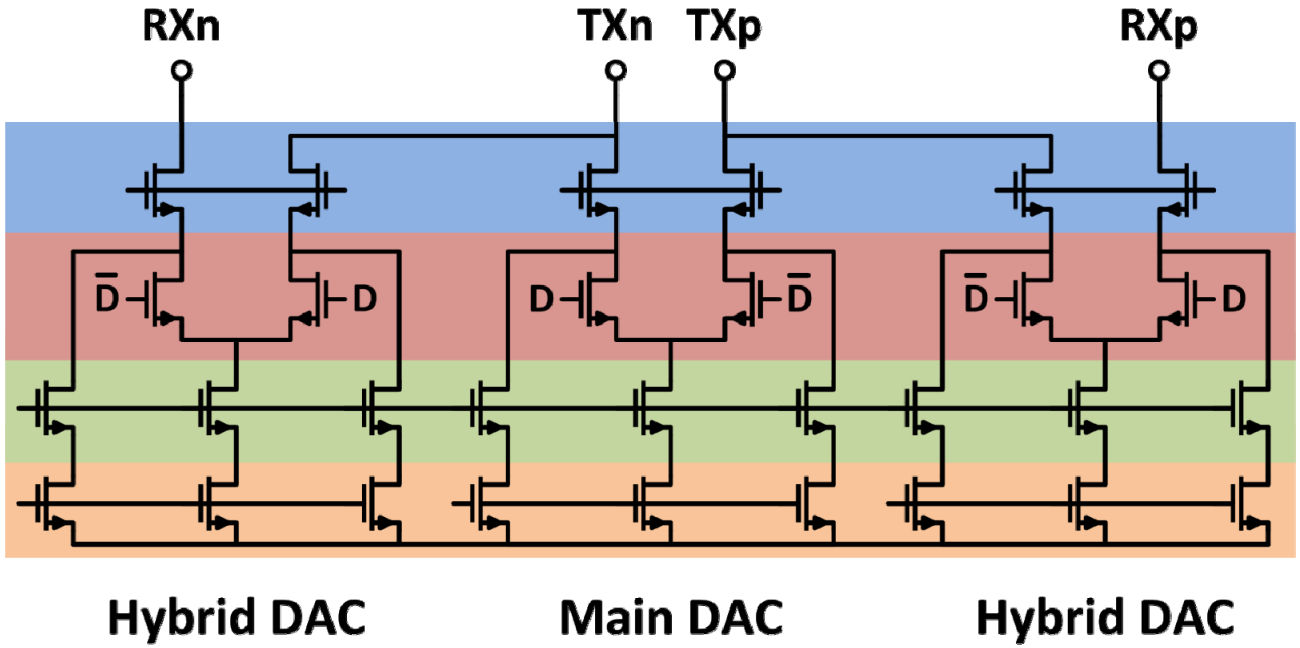
12-bit 6+6 segmented current DAC



TX / Hybrid Architecture

12-bit 6+6 segmented current DAC

‘Always-on’ cascodes for high linearity

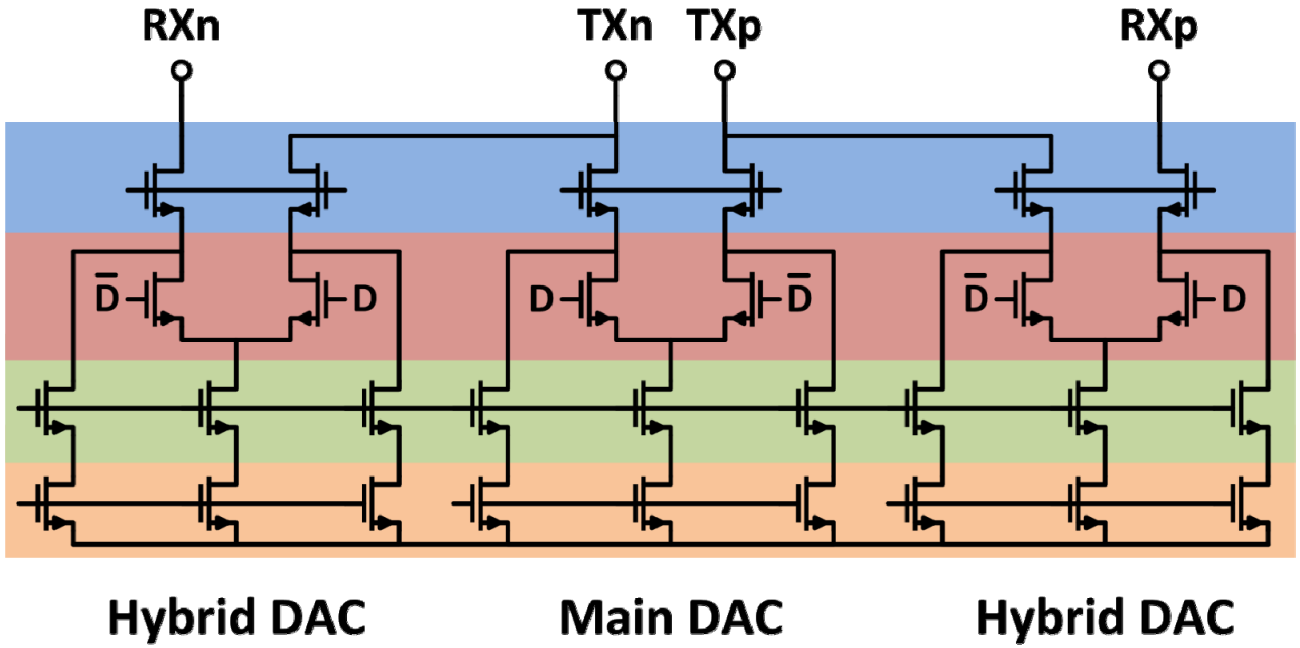


TX / Hybrid Architecture

12-bit 6+6 segmented current DAC

'Always-on' cascodes for high linearity

Clocked at 1.6GS/s (2 x symbol rate)



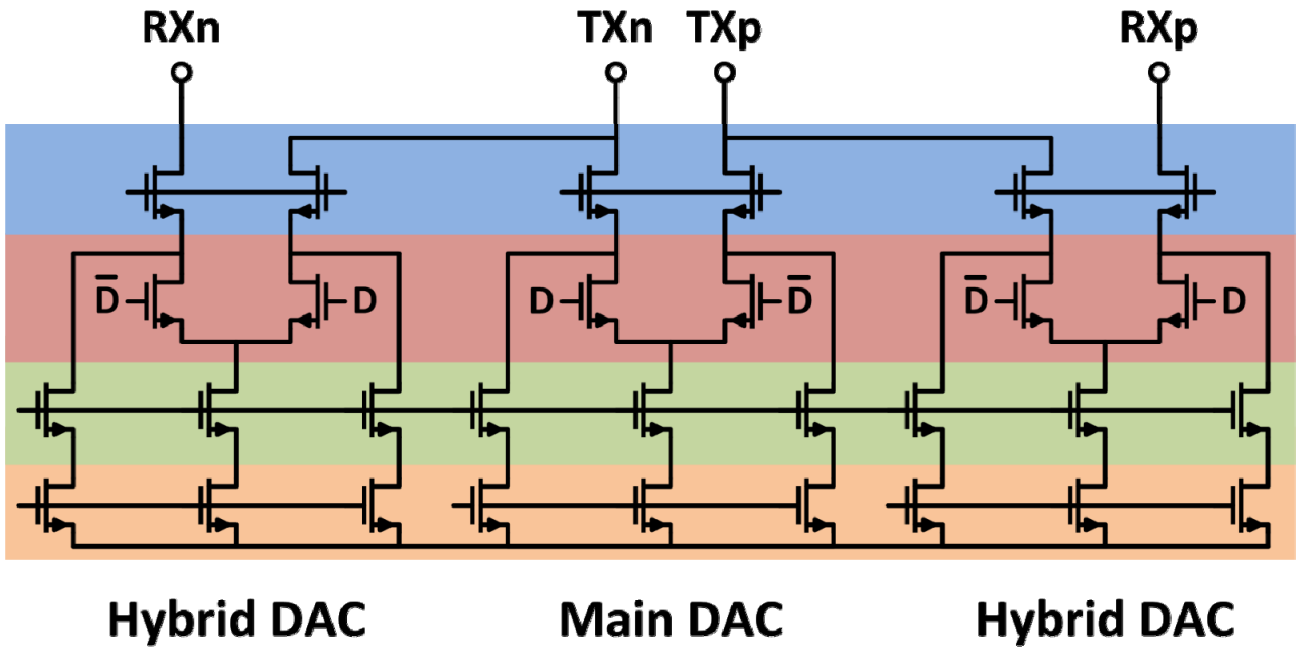
TX / Hybrid Architecture

12-bit 6+6 segmented current DAC

'Always-on' cascodes for high linearity

Clocked at 1.6GS/s (2 x symbol rate)

Filter out-of-band CM for low EMI



TX / Hybrid Architecture

12-bit 6+6 segmented current DAC

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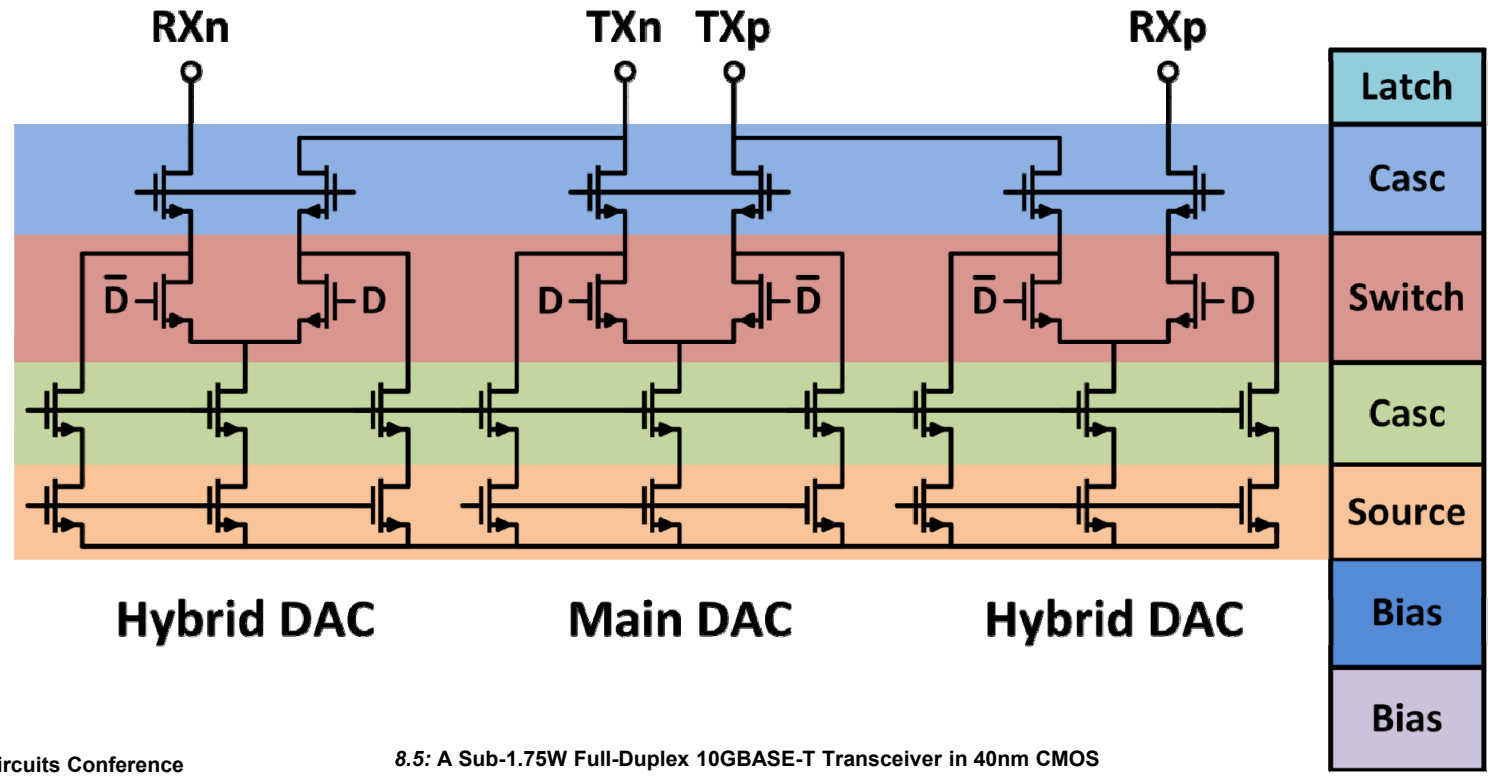
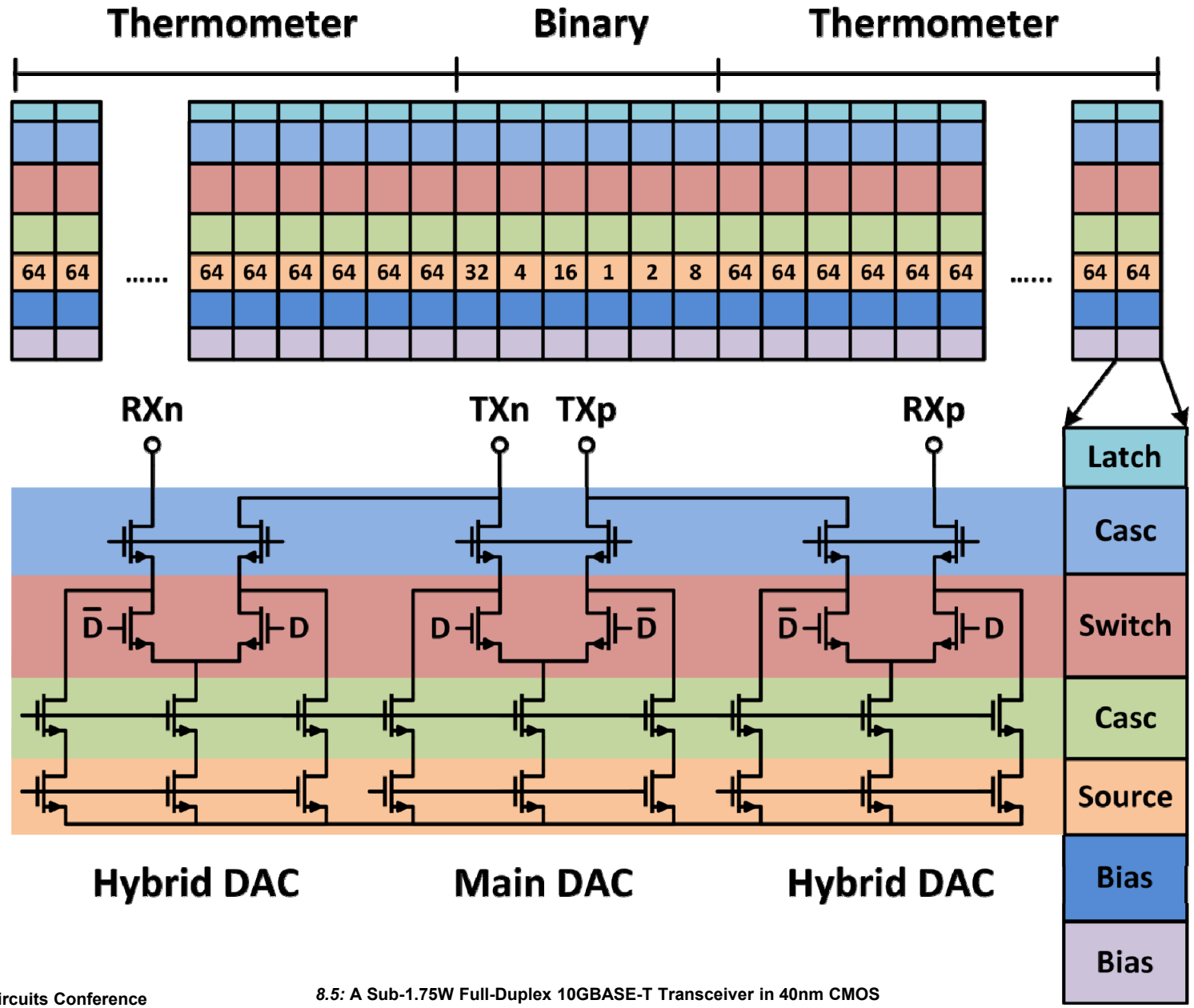
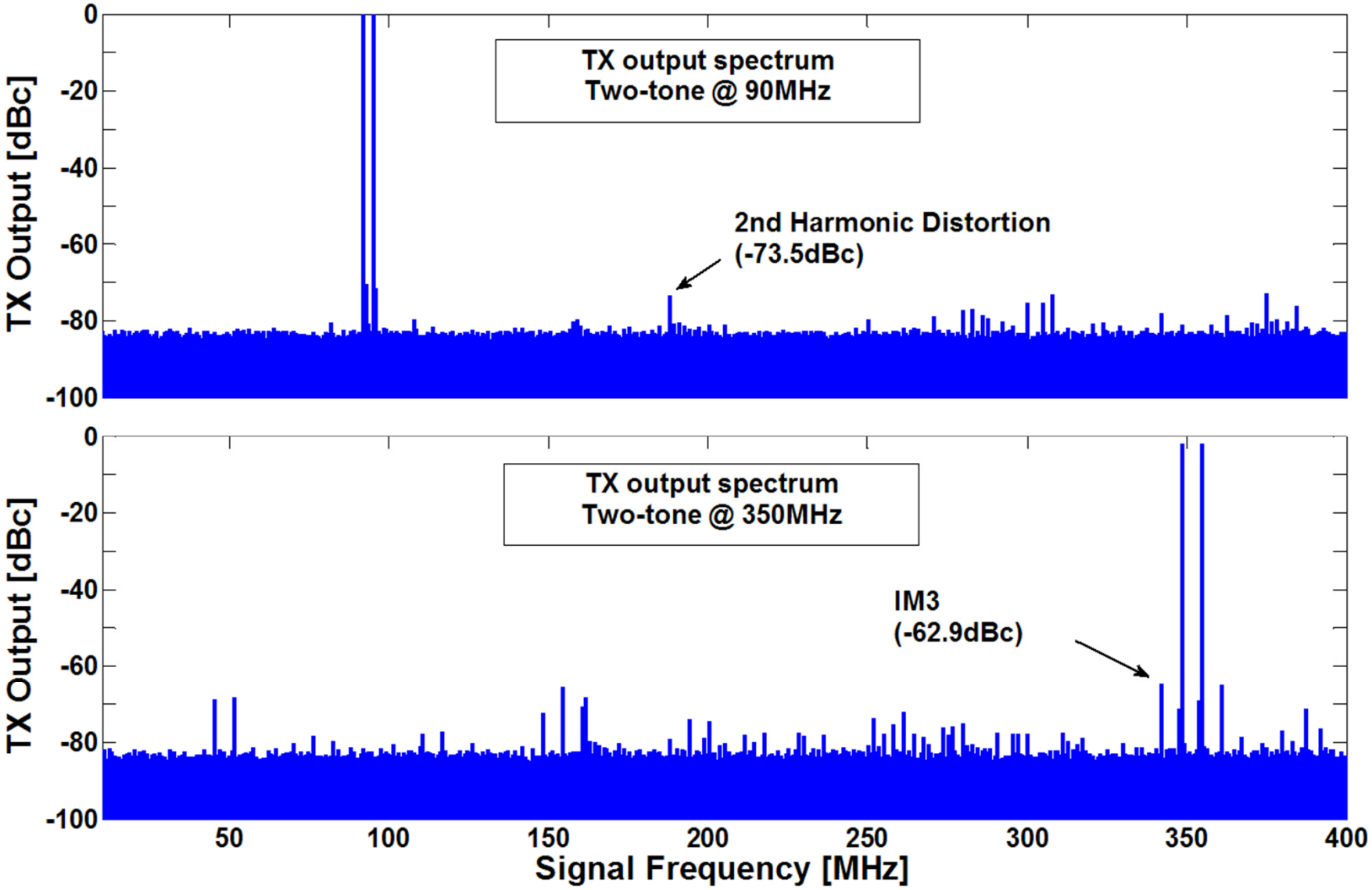


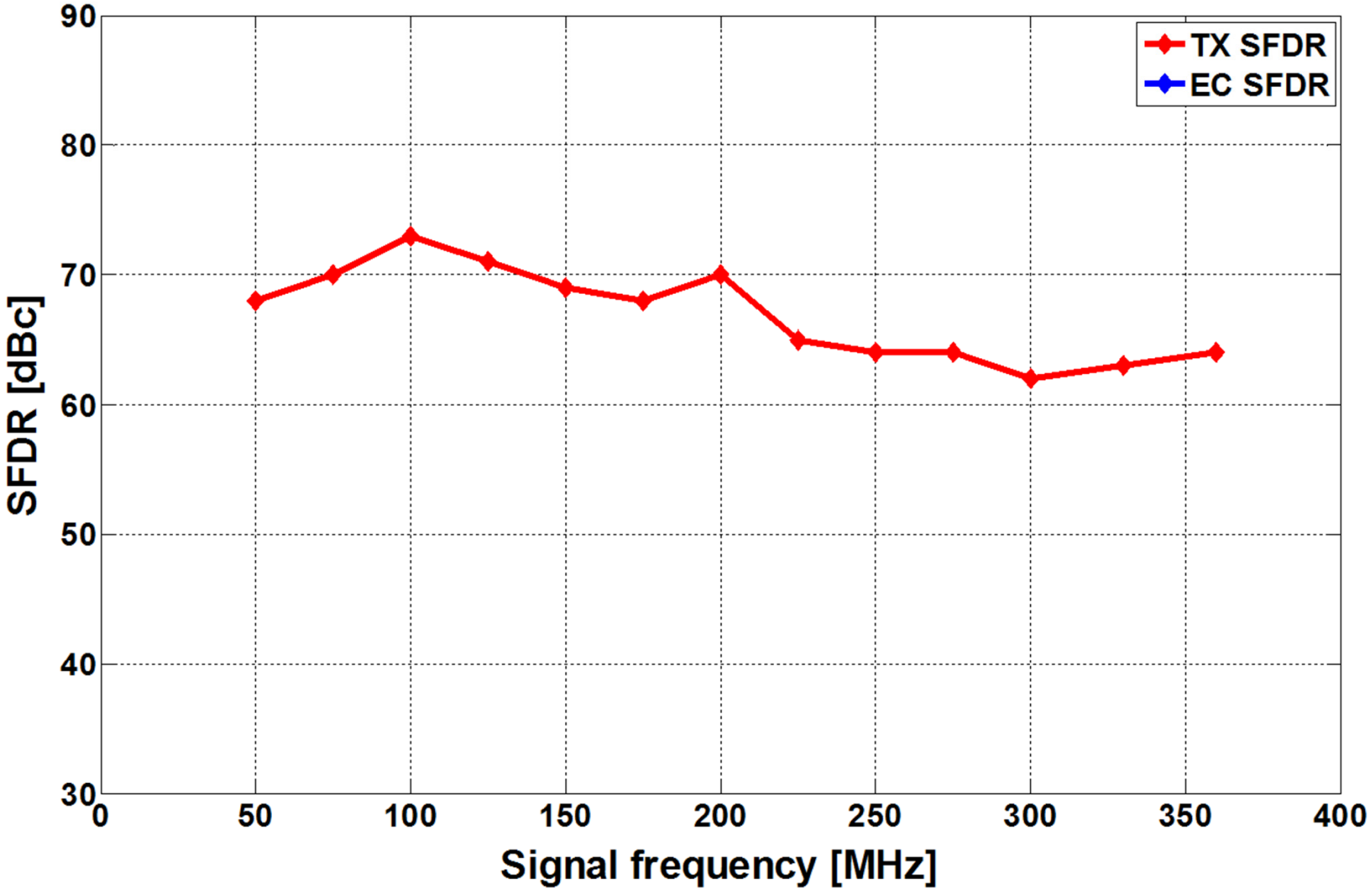
TX / Hybrid Architecture



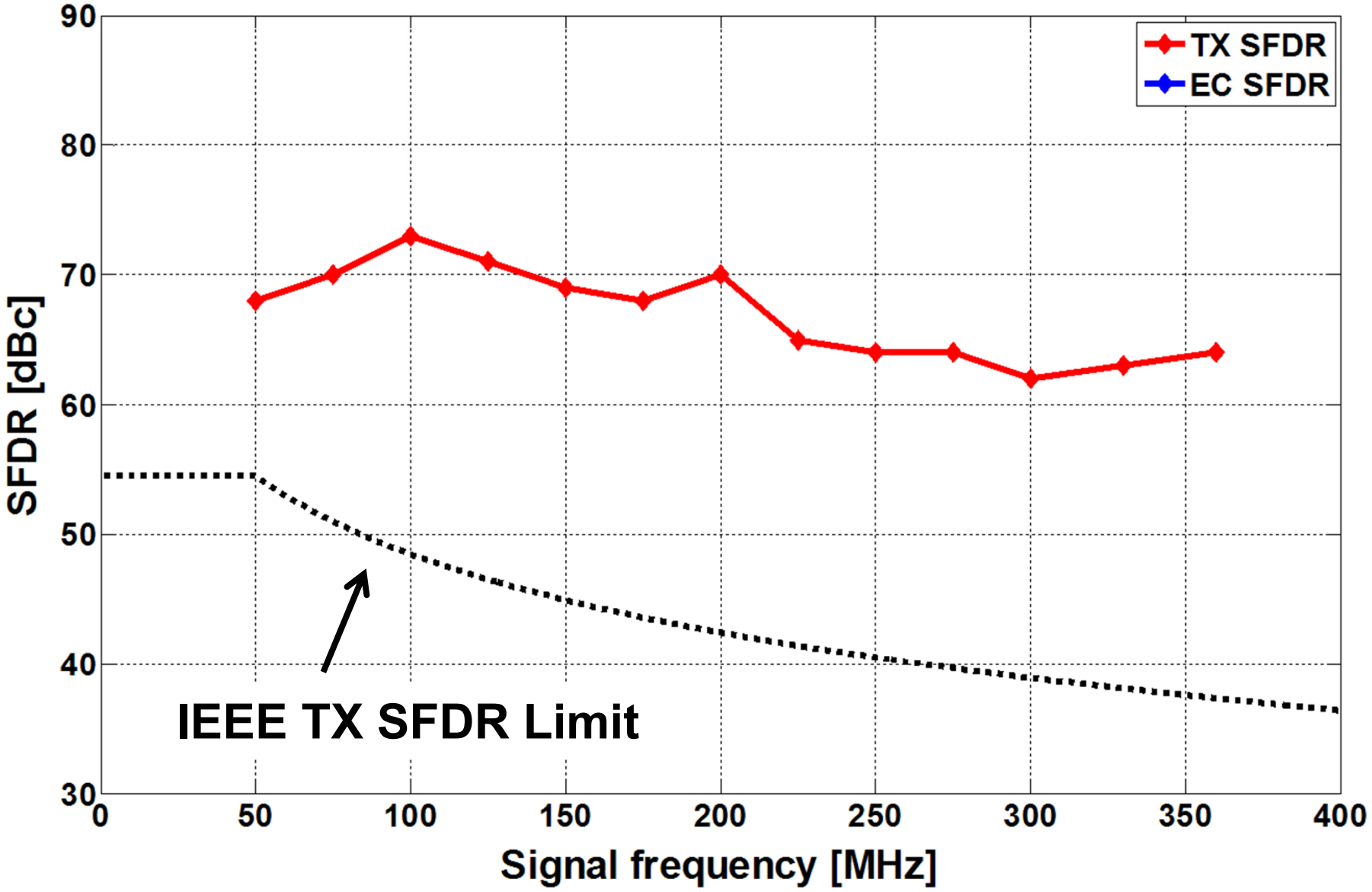
TX SFDR



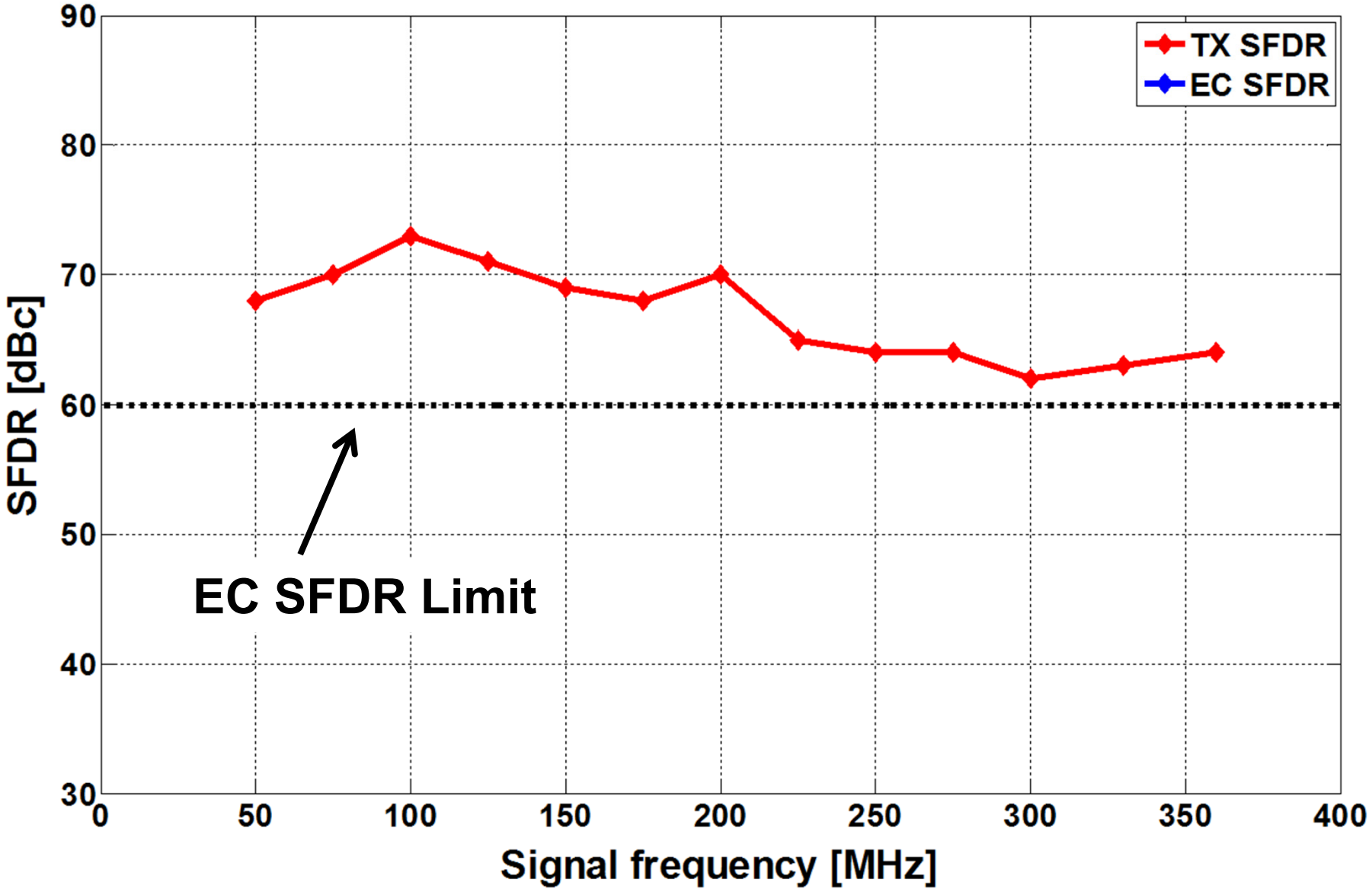
TX / Hybrid SFDR



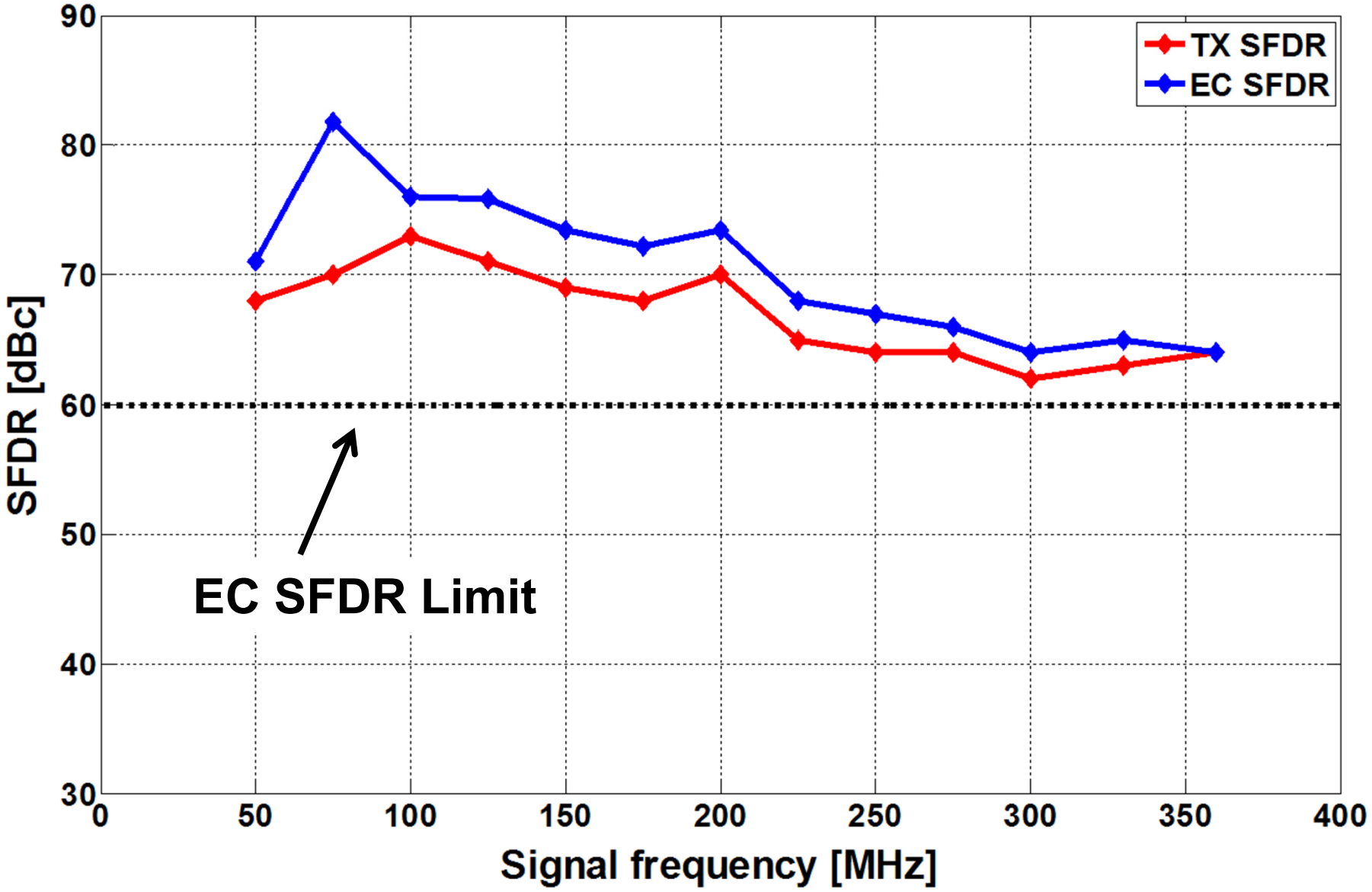
TX / Hybrid SFDR



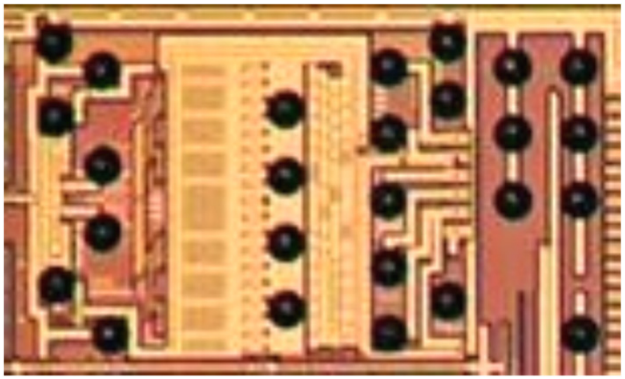
TX / Hybrid SFDR



TX / Hybrid SFDR

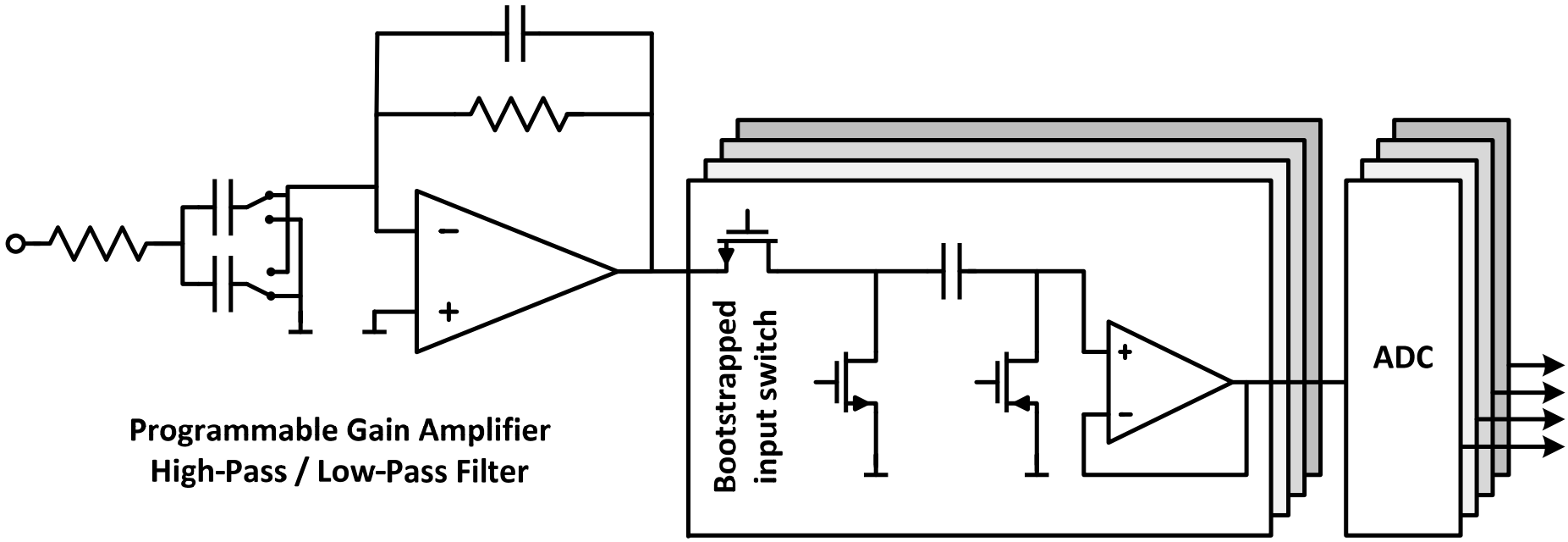


TX / Hybrid Summary

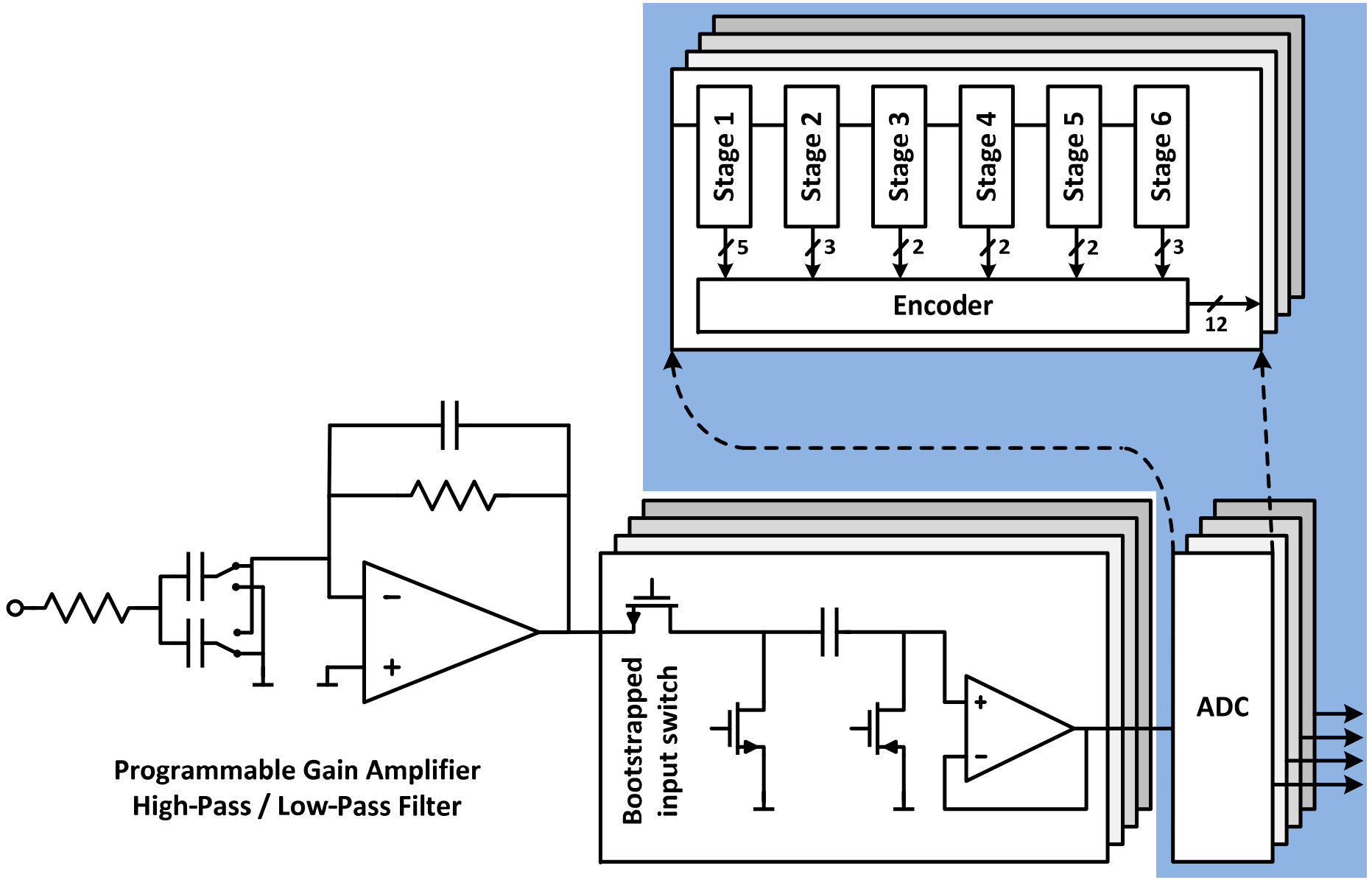


Parameter	Value
TX input	12b @ 1.6GS/s
Transmitter linearity	> 62dBc
Hybrid Cancellation	> 20dB (<200MHz), >10dB (<400MHz)
Supply Voltage	1V / 2.5V
TX / Hybrid Area	1.5mm^2
TX Power	160mW
Hybrid Power	40mW
Total Power	200mW

Receiver Architecture

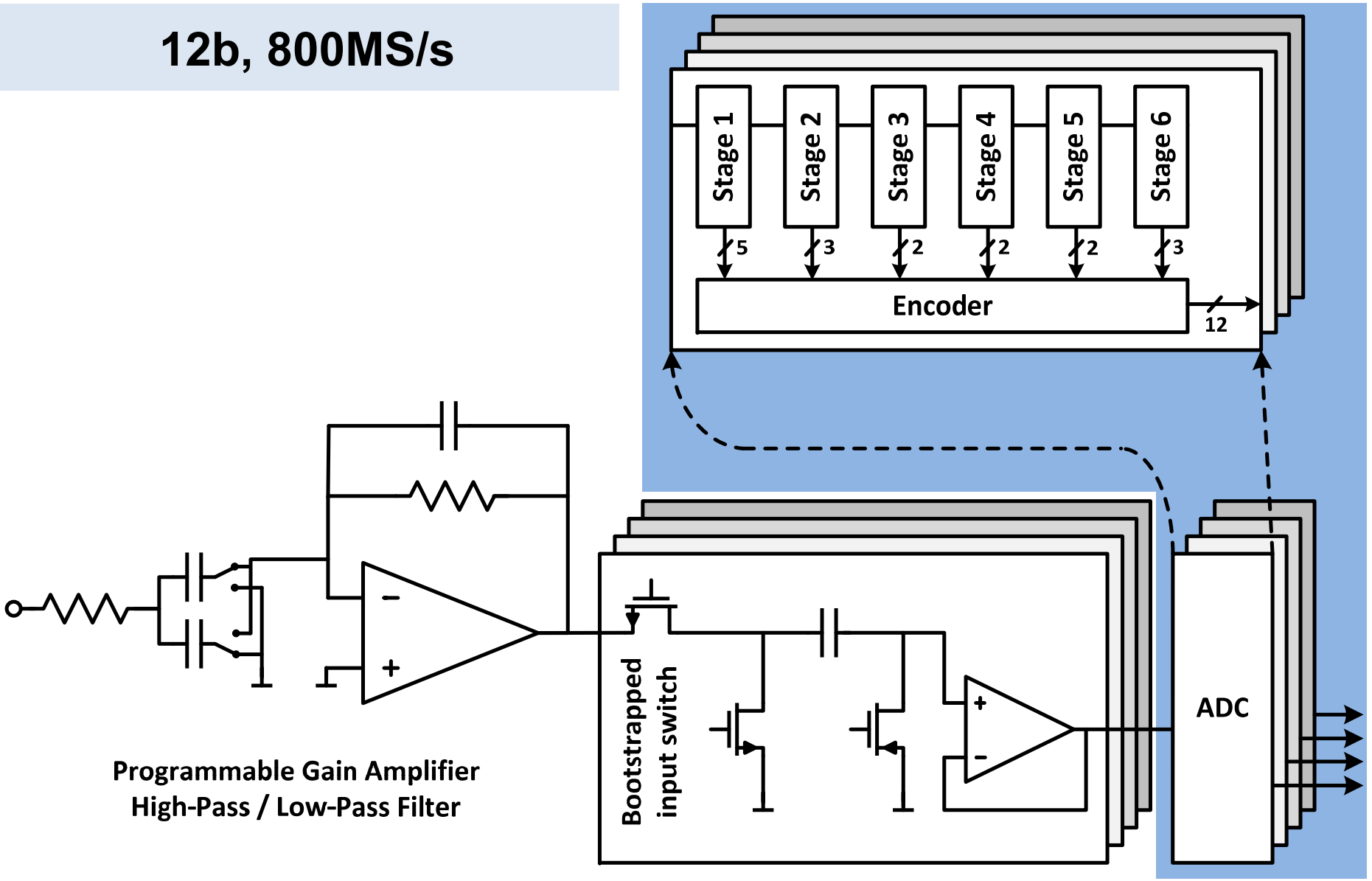


Receiver Architecture



Receiver Architecture

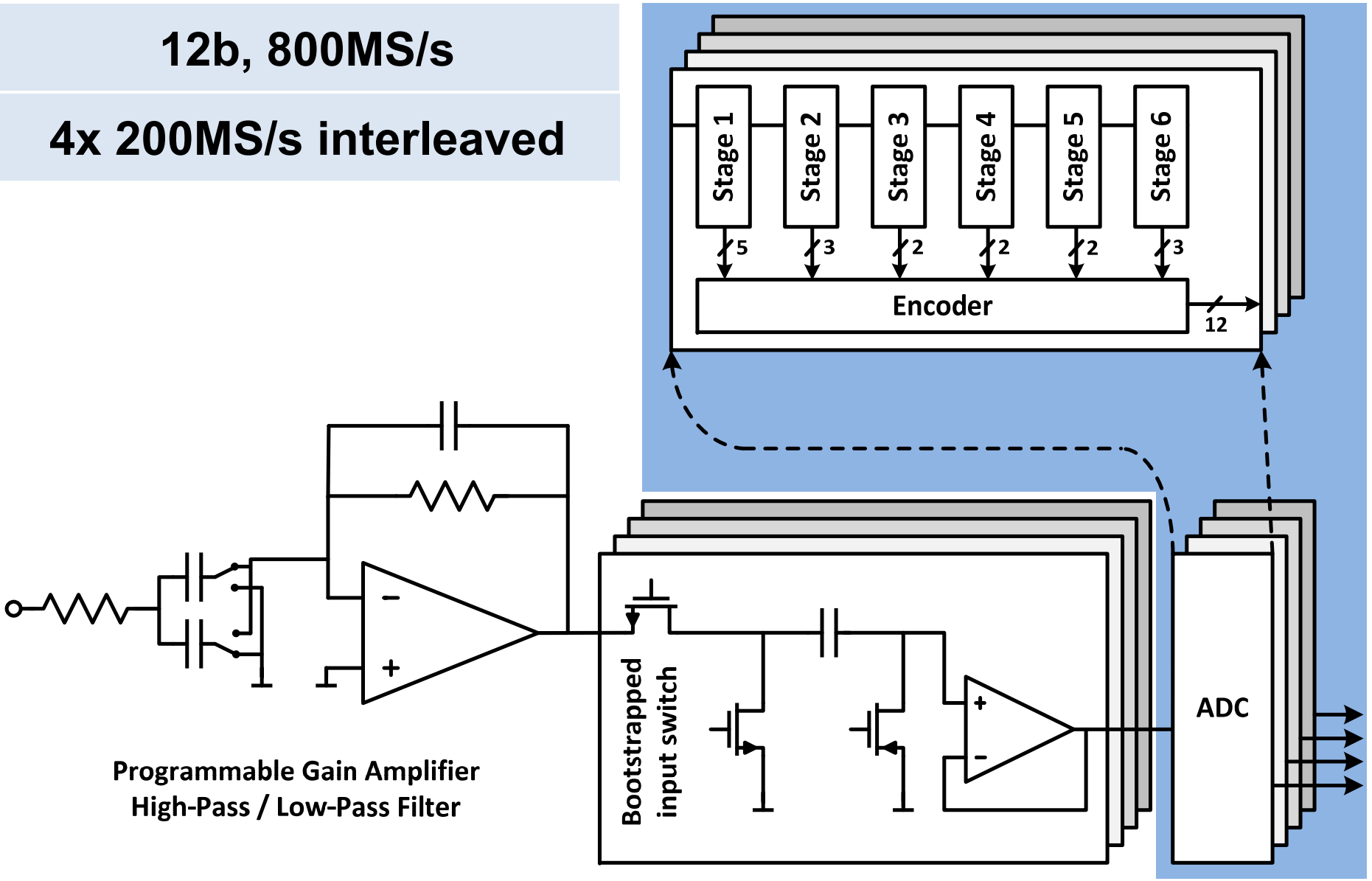
12b, 800MS/s



Receiver Architecture

12b, 800MS/s

4x 200MS/s interleaved

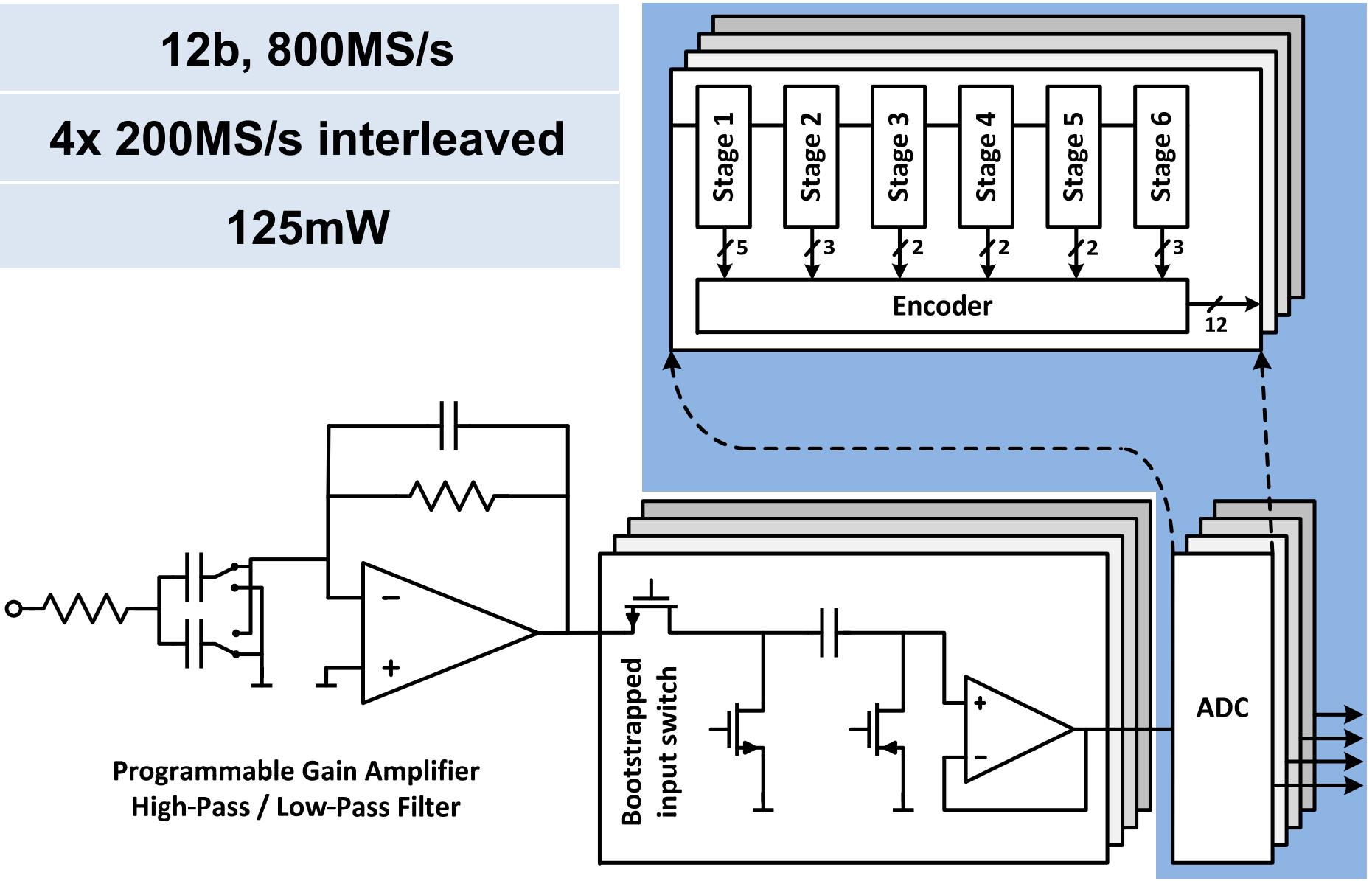


Receiver Architecture

12b, 800MS/s

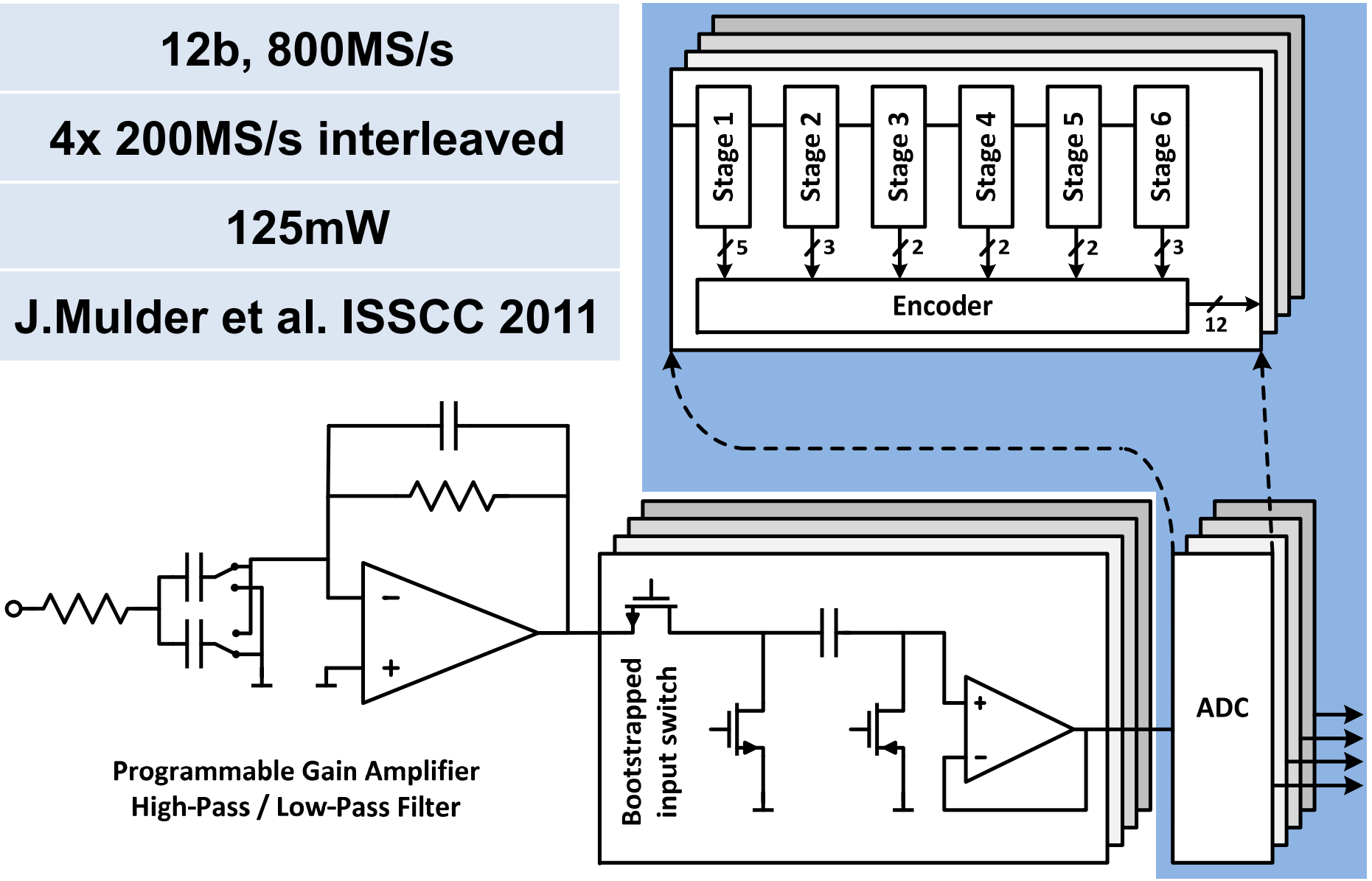
4x 200MS/s interleaved

125mW

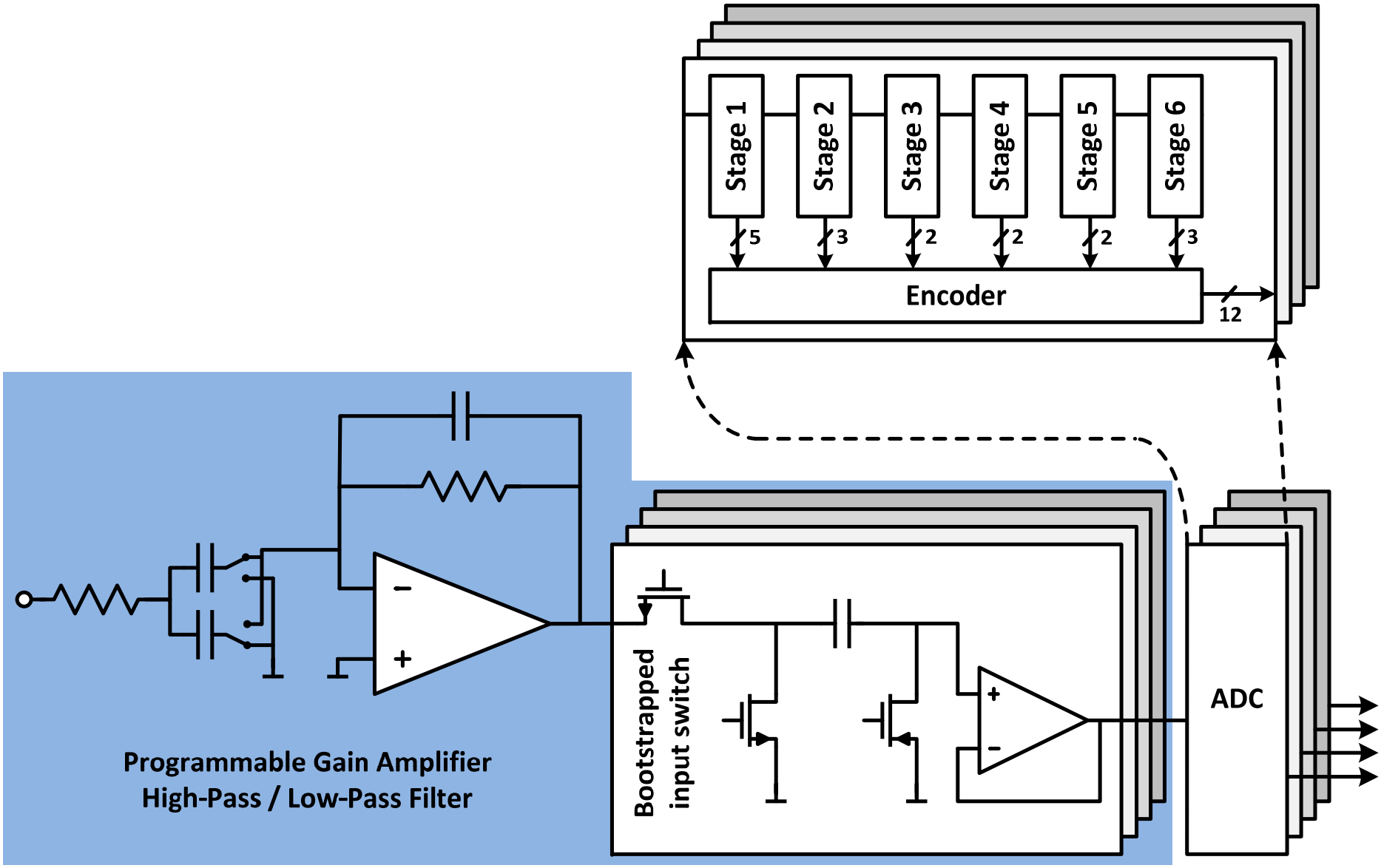


Receiver Architecture

- 12b, 800MS/s
- 4x 200MS/s interleaved
- 125mW
- J.Mulder et al. ISSCC 2011

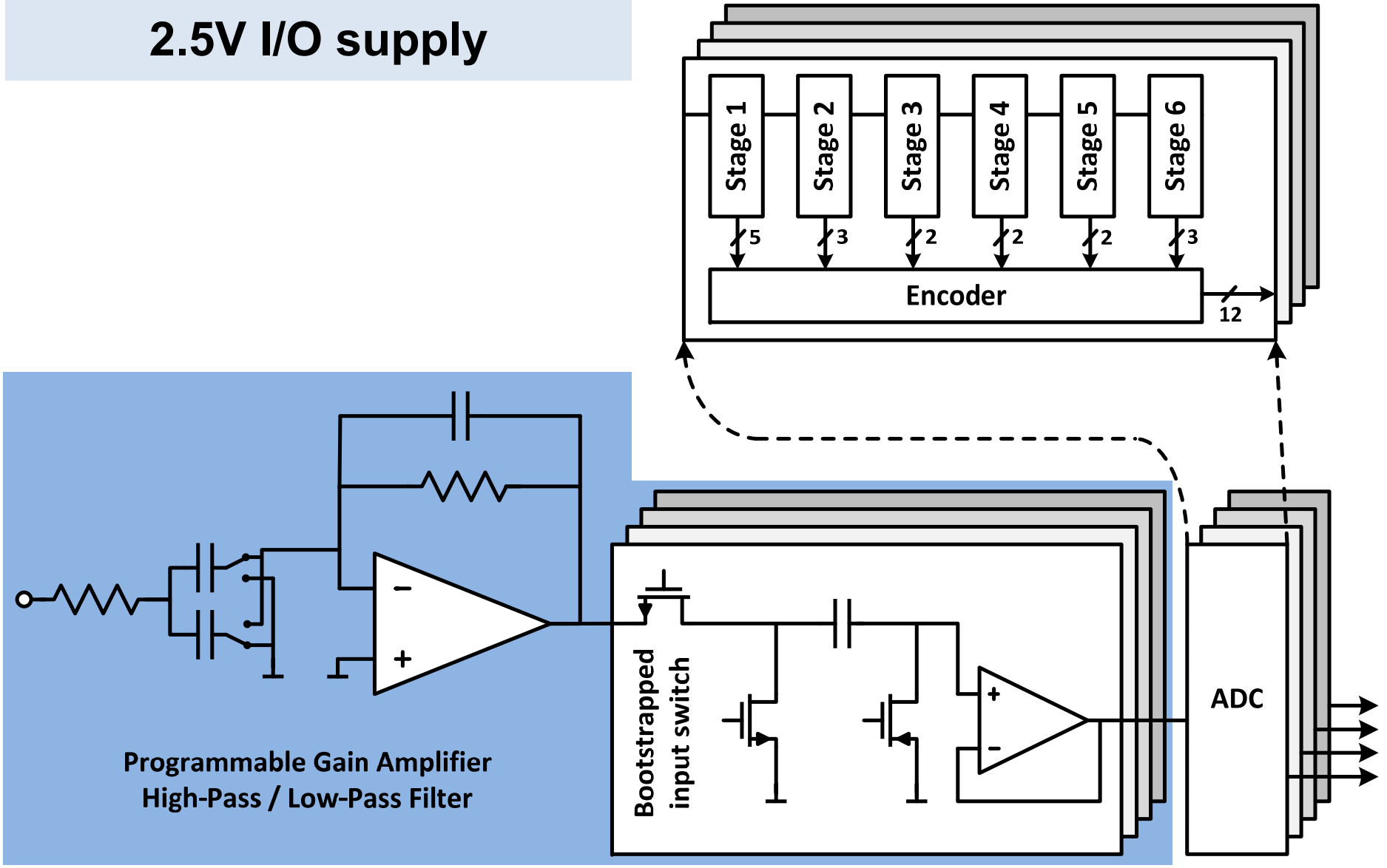


Receiver Architecture



Receiver Architecture

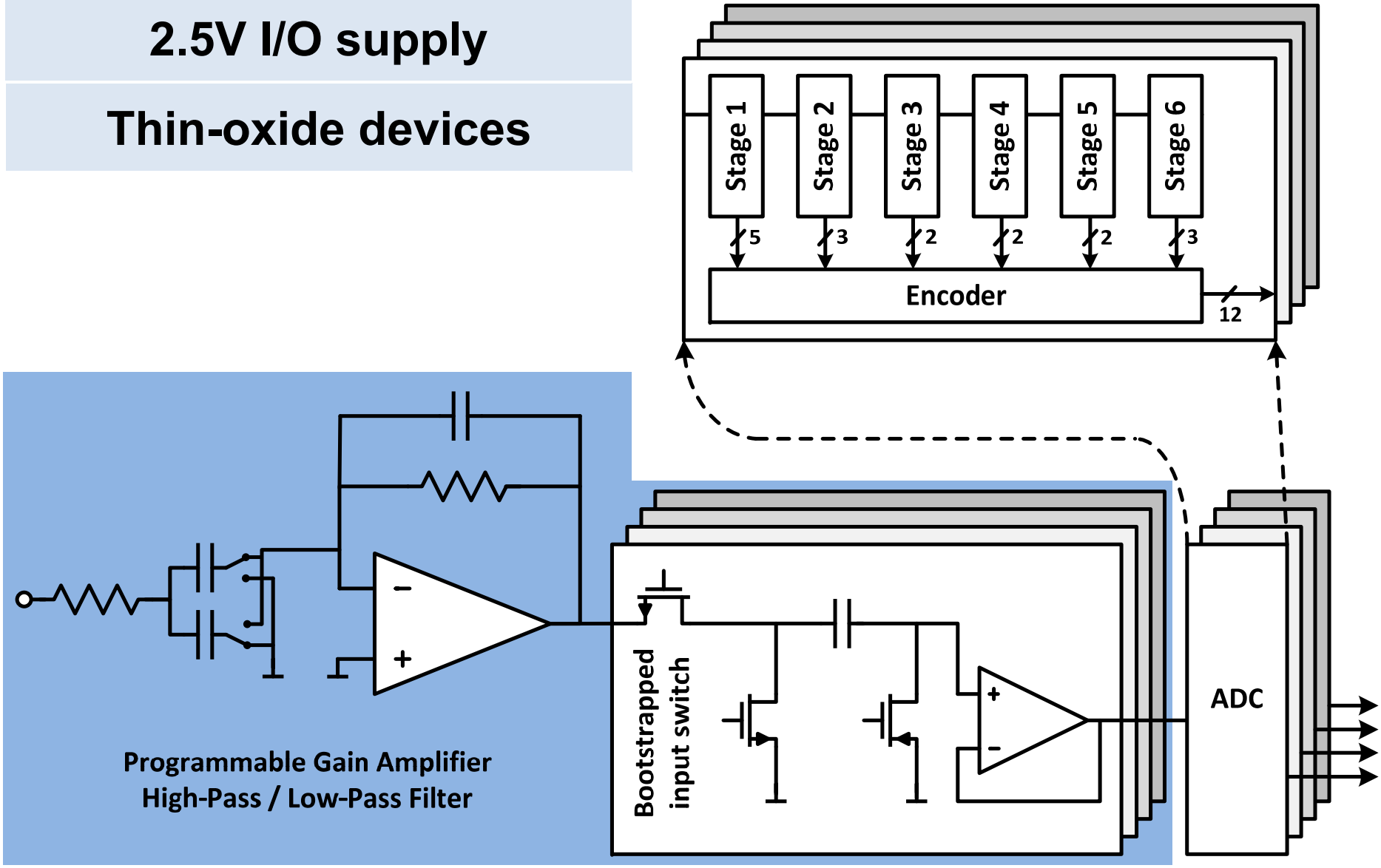
2.5V I/O supply



Receiver Architecture

2.5V I/O supply

Thin-oxide devices

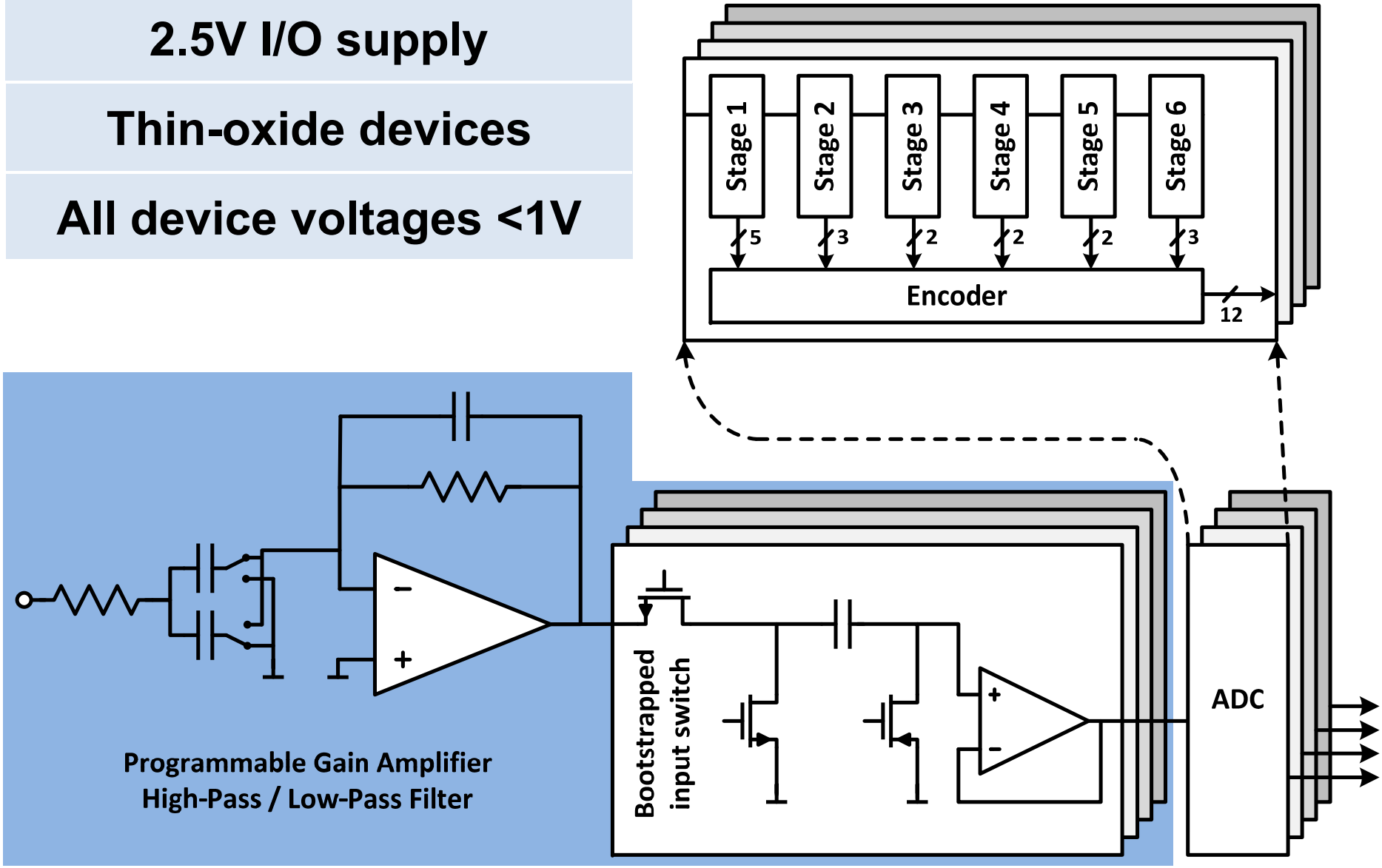


Receiver Architecture

2.5V I/O supply

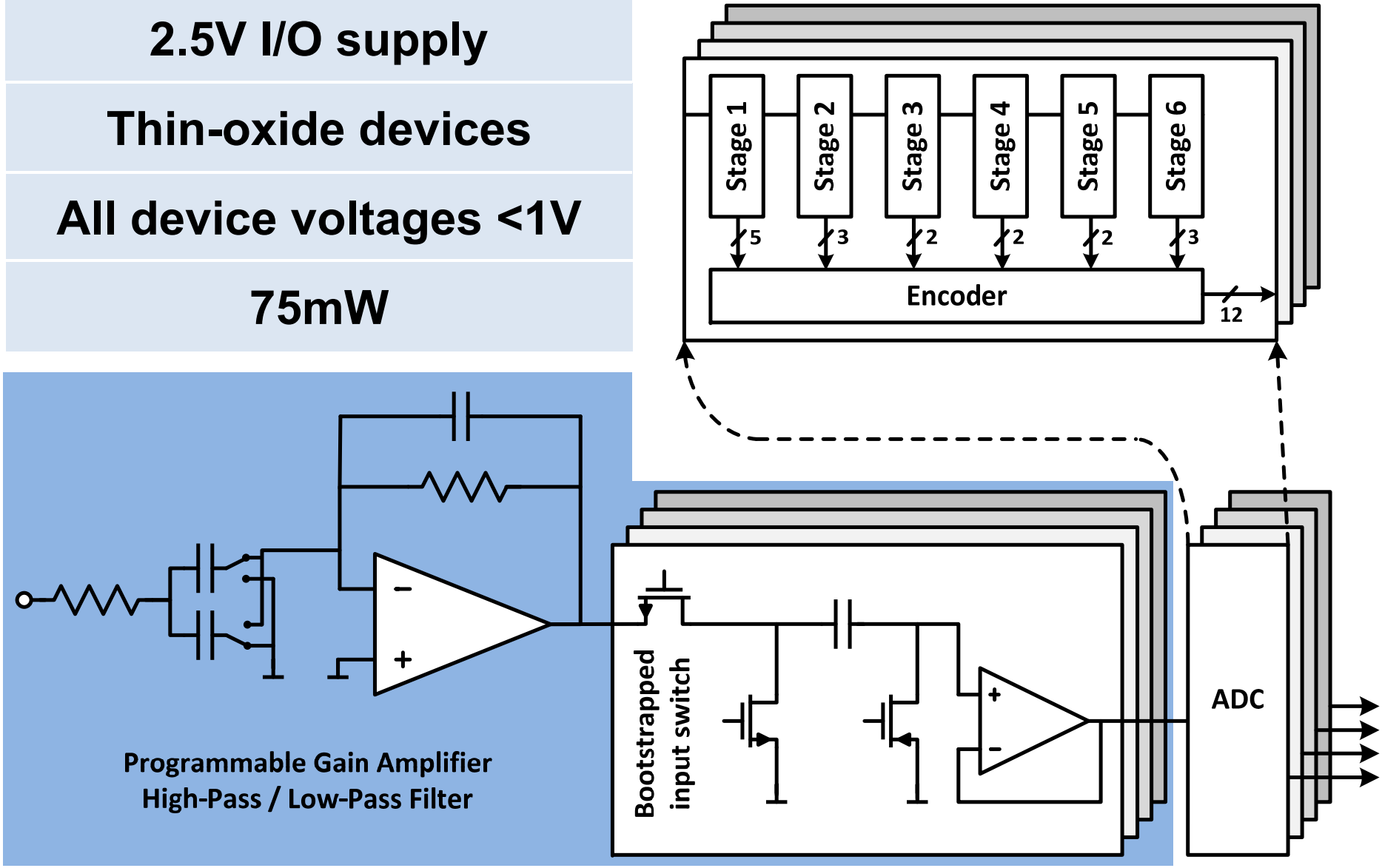
Thin-oxide devices

All device voltages <1V

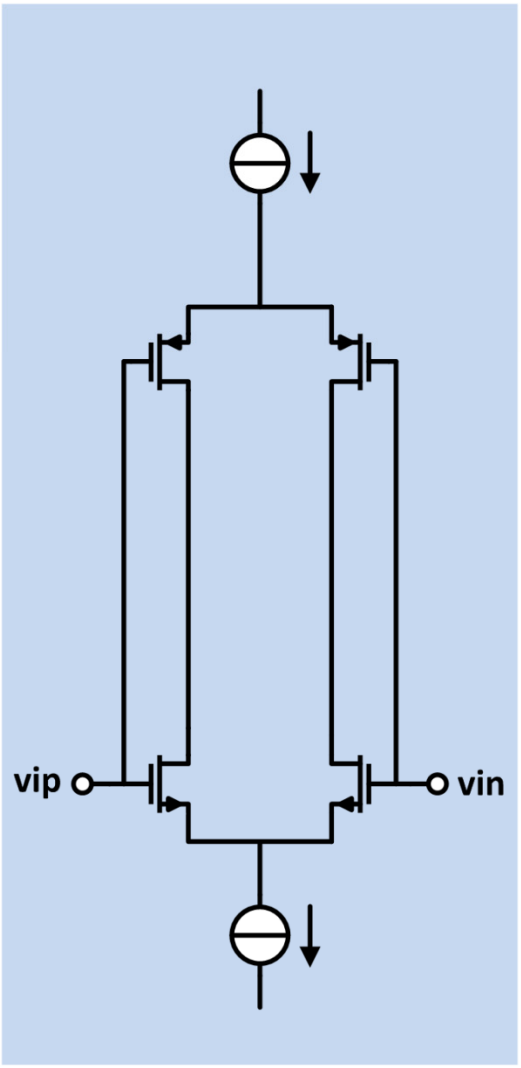


Receiver Architecture

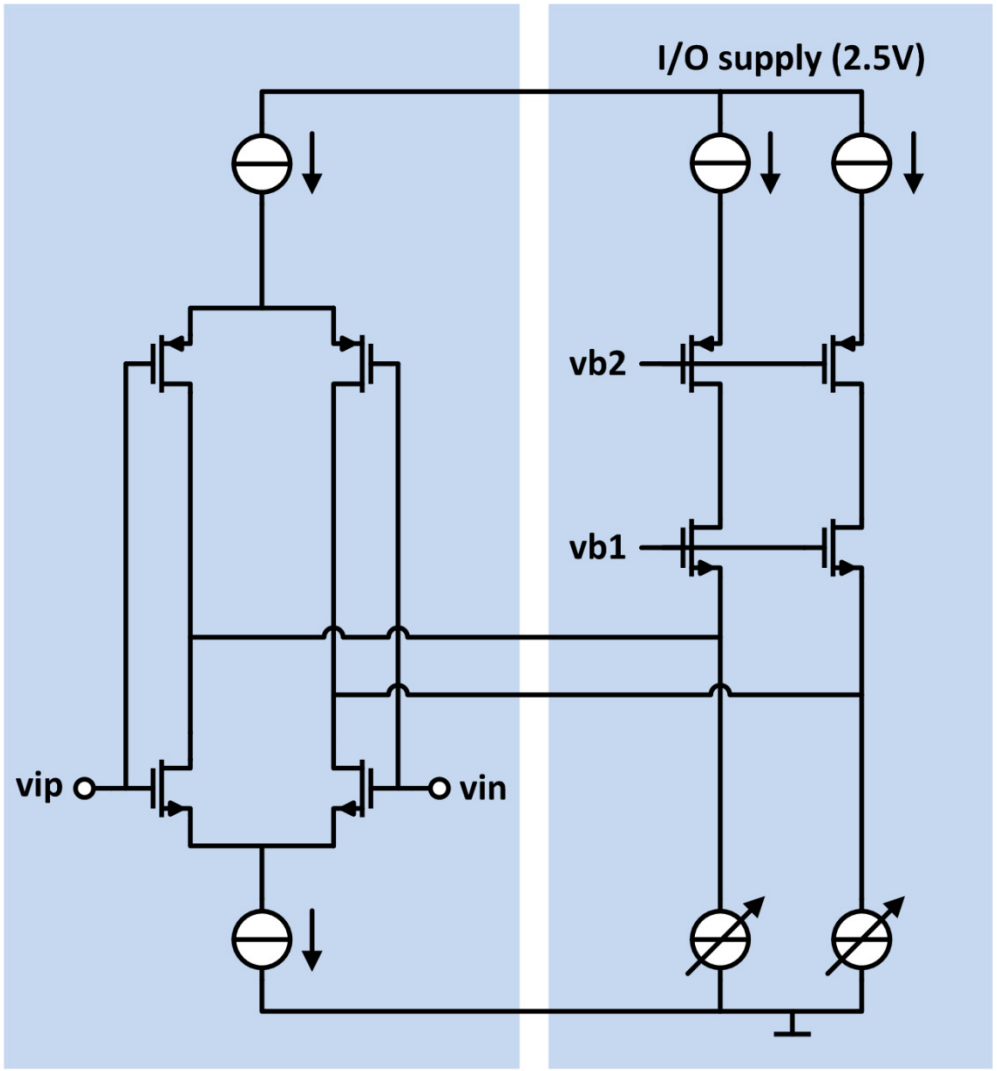
- 2.5V I/O supply
- Thin-oxide devices
- All device voltages <1V
- 75mW



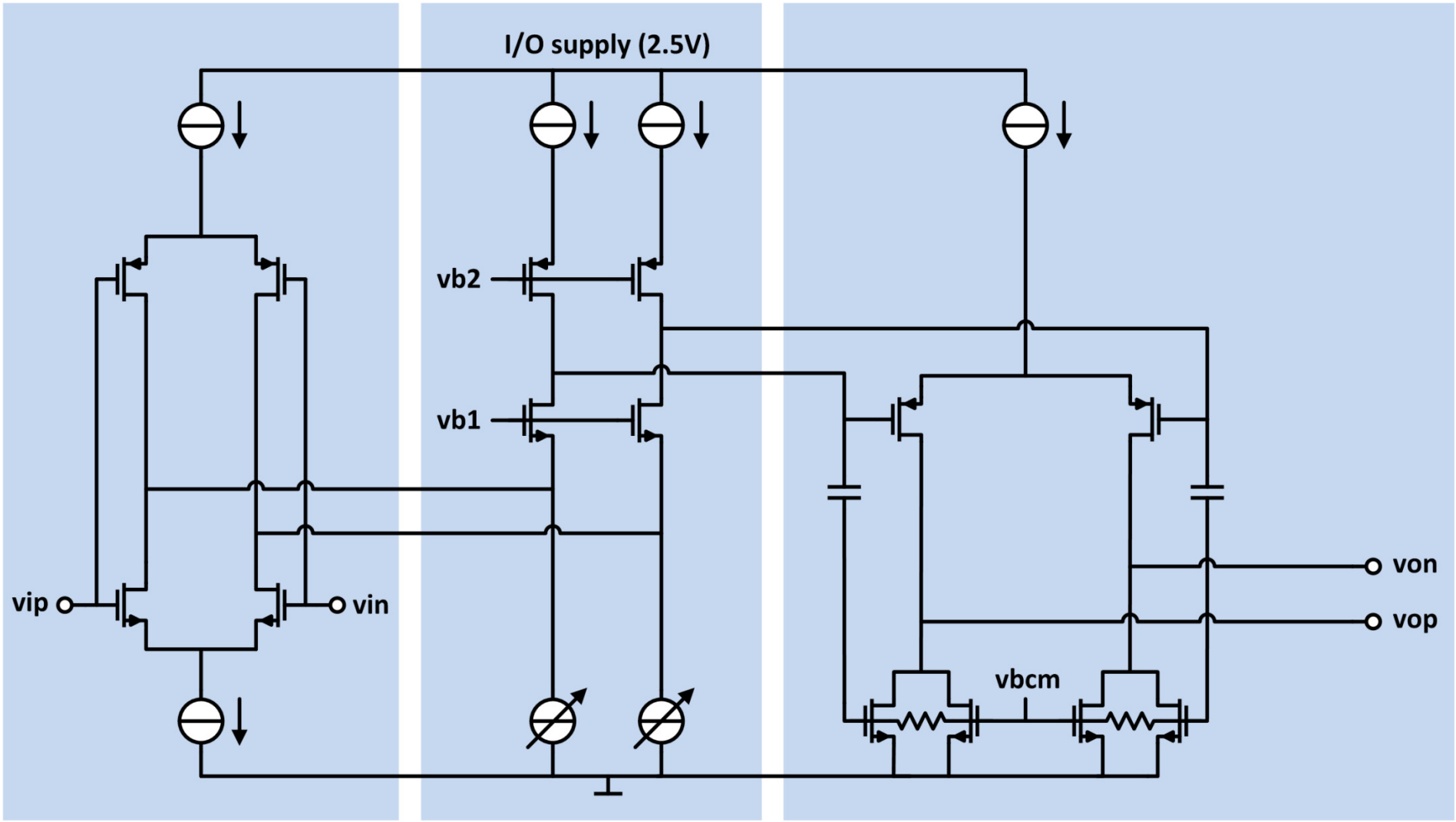
Programmable Gain Amplifier



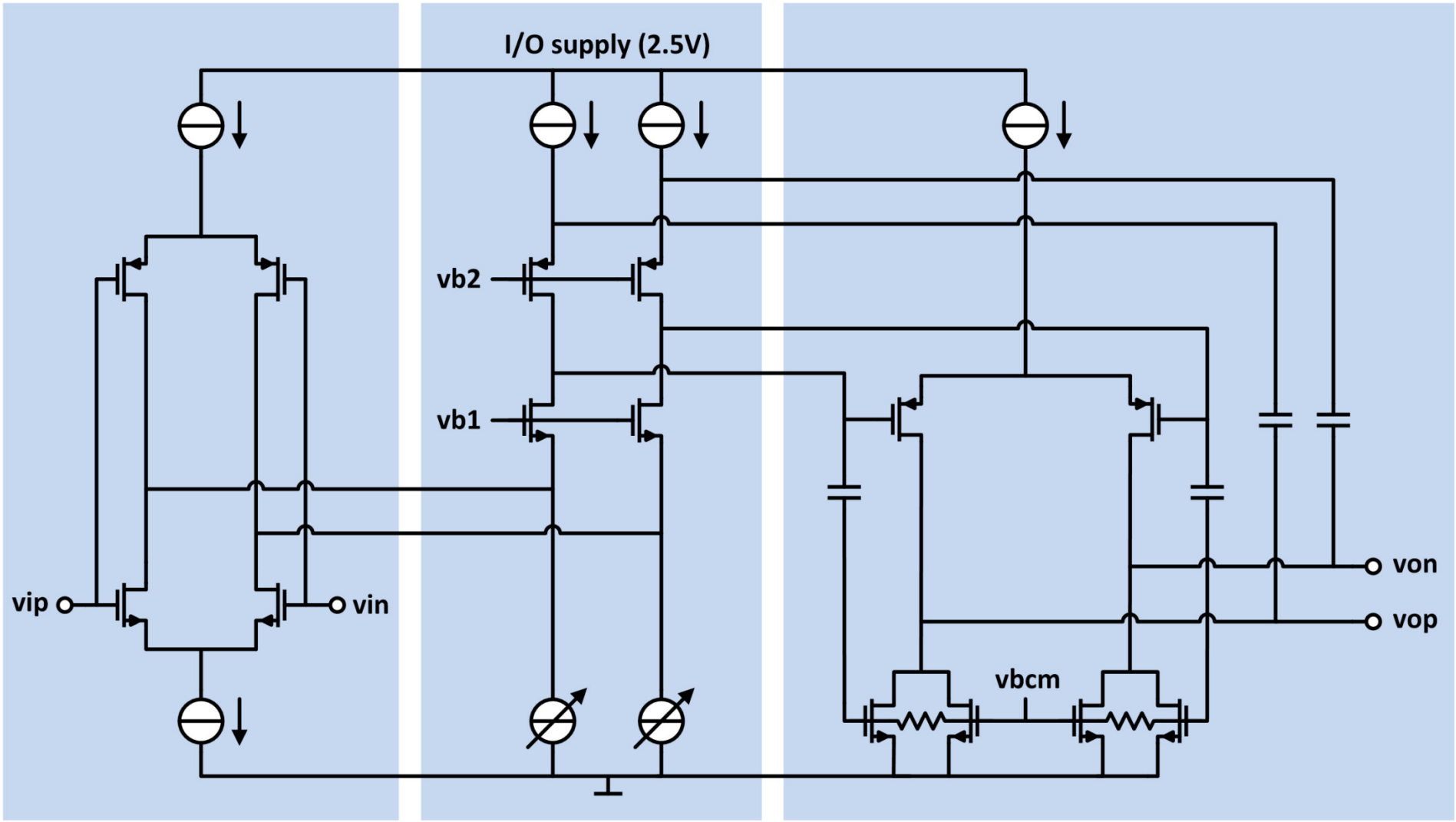
Programmable Gain Amplifier



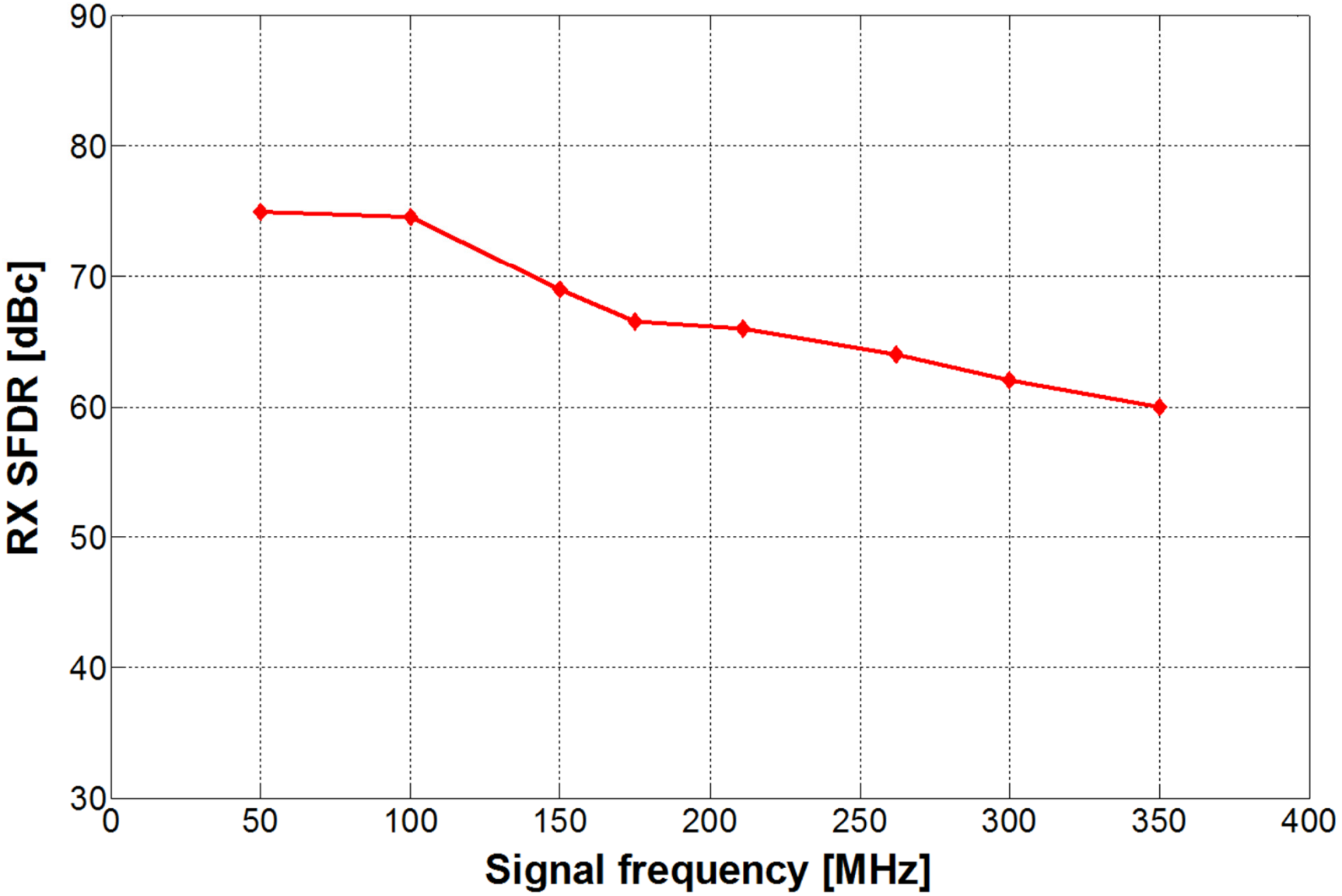
Programmable Gain Amplifier



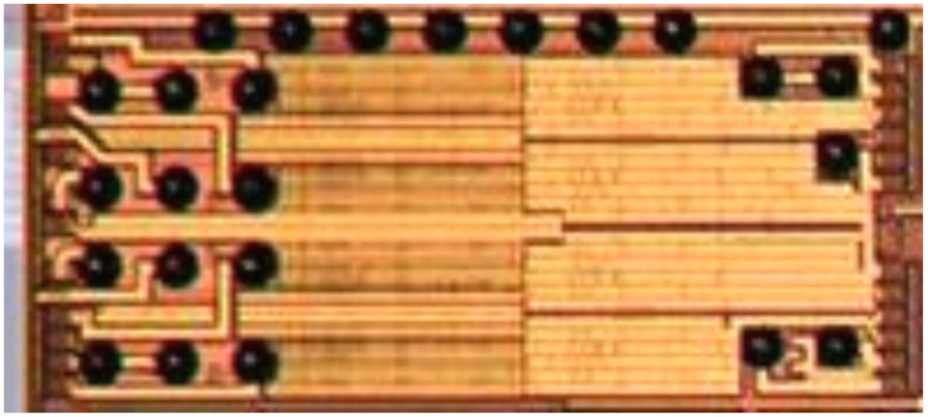
Programmable Gain Amplifier



RX SFDR

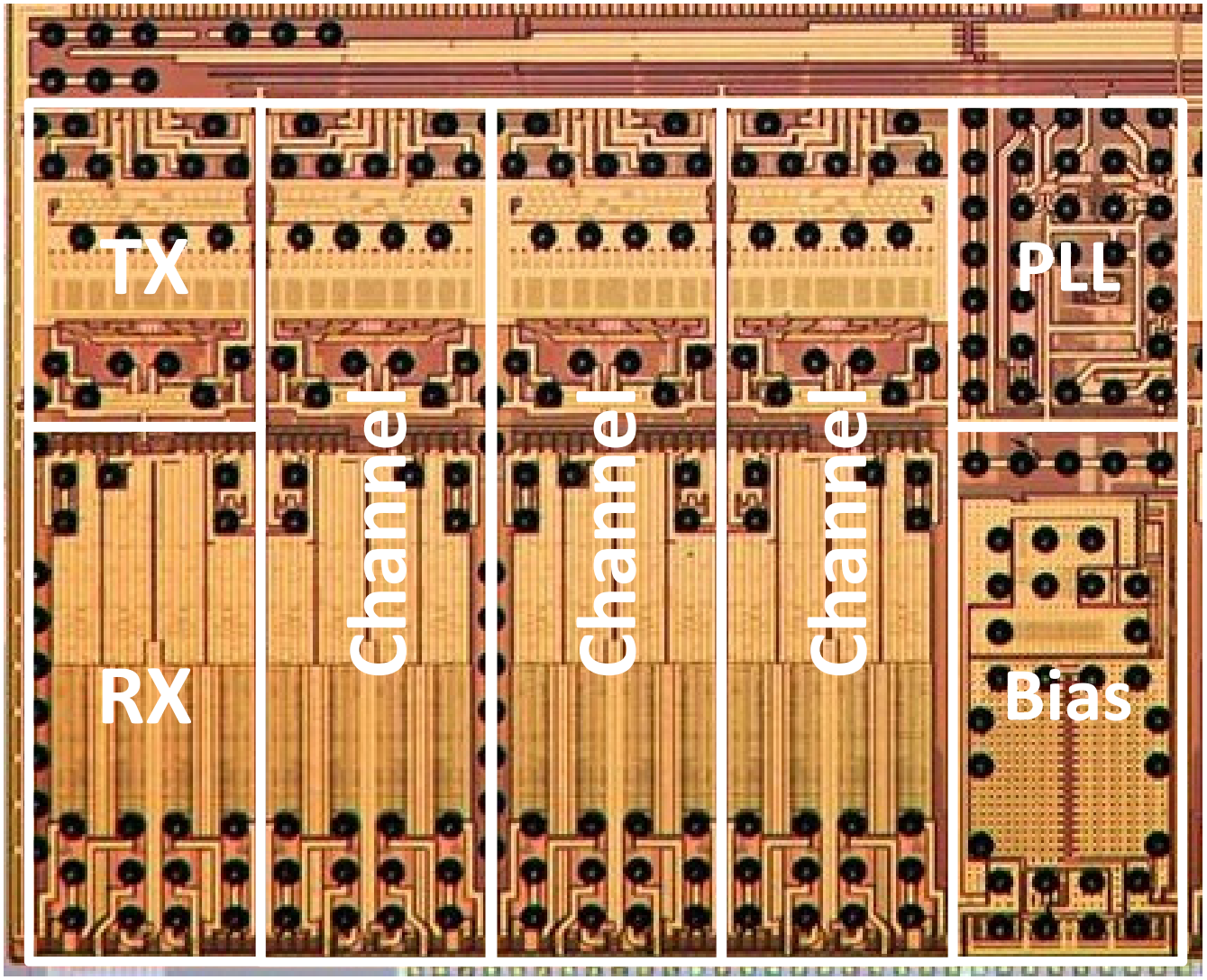


RX Summary

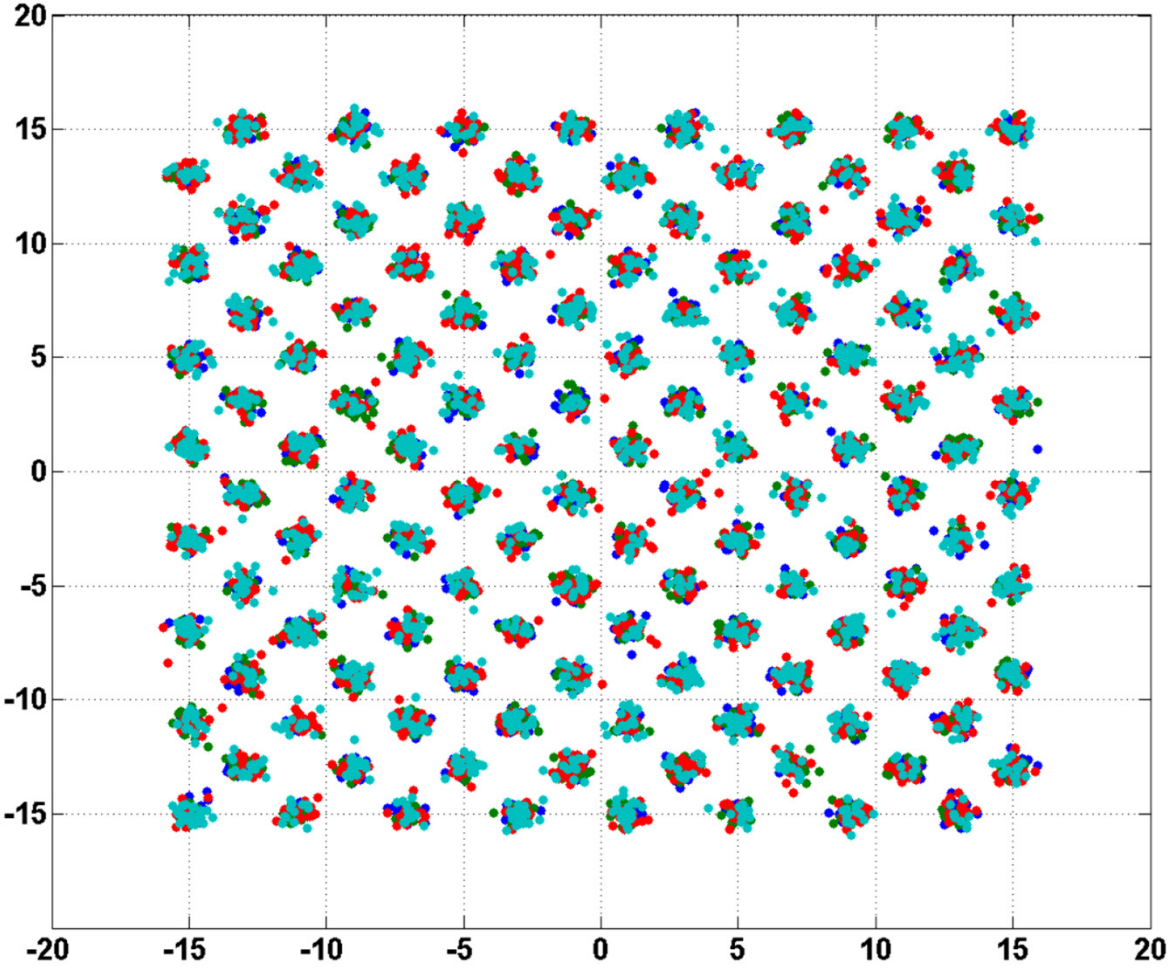


Parameter	Value
Output bits	12
Sample Frequency	800MS/s (4x interleaved)
RX linearity	> 60dBc
RX ENOB	> 10
Supply Voltage	1V / 2.5V
RX Area	2.2mm^2
RX Power	200mW

Micrograph



Receiver Constellation



128 DSQ Constellation over 100m, after DSP, before LDPC

SNR > 28.5dB, BER<10^{-15} (spec for BER 10^{-12}: 23.5dB)

State-of-the-Art

Parameter	T. Gupta et.al. [ISSCC 2012]	This Work
TX SFDR	> 59dB	> 62dB
RX SFDR	> 53dB	> 60dB
Slicer SNR	> 27.5dB	> 28.5dB
Receiver noise Floor	< -144dBm/Hz	< -147dBm/Hz
Process Technology	Triple gate ox 40nm	Dual gate ox 40nm
Supply Voltage	0.9V / 1.2V / 2.5V	1.0V / 2.5V
AFE Area	17mm^2	15.5mm^2
AFE Power	< 2W	< 1.75W

Conclusions

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Echo cancellation linearity is a key enabler for 10GBASE-T

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Transmitter linearity greatly enhances robustness

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Robust, lowest power 10GBASE-T AFE in 40nm CMOS

A Full-Duplex Line Driver for Gigabit Ethernet with Rail-to-Rail Class-AB Output Stage in 28nm CMOS

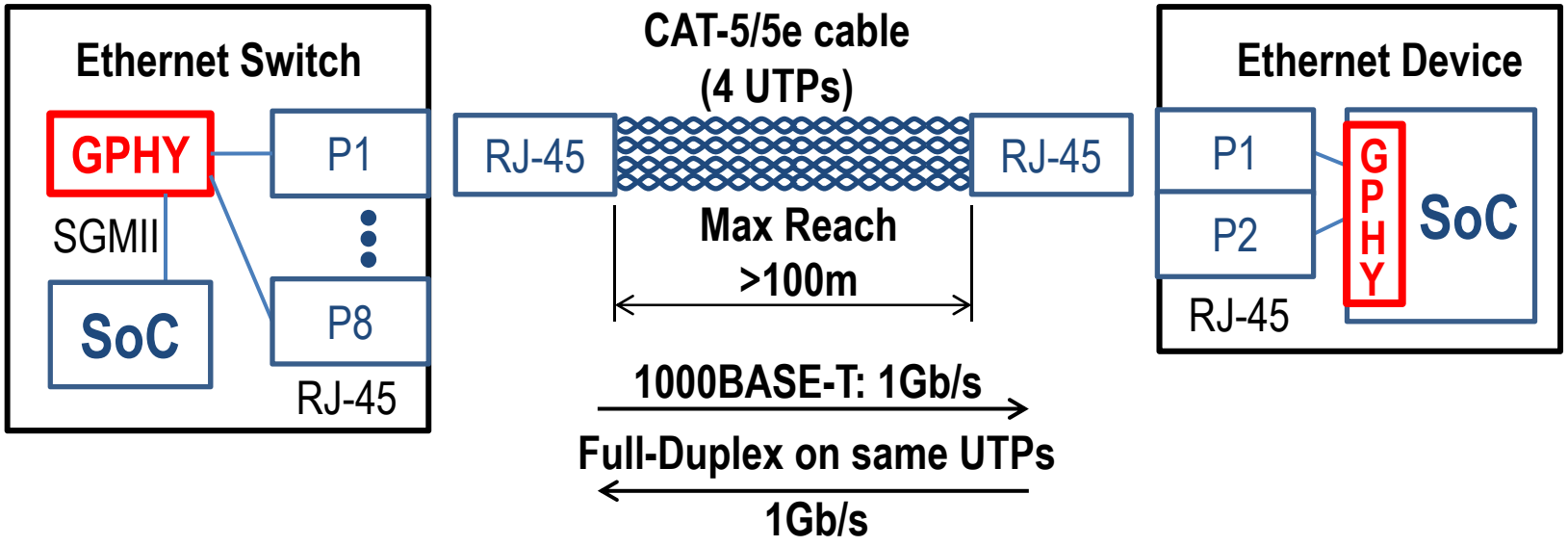
Hui Pan, Yuan Yao, Mostafa Hammad, Junhua Tan,
Karim Abdelhalim, Evelyn Wang, Rick Hsu, Jenny Yu,
Joseph Aziz, Derek Tam, Ichiro Fujimori

Broadcom Corporation, Irvine, CA

Outline

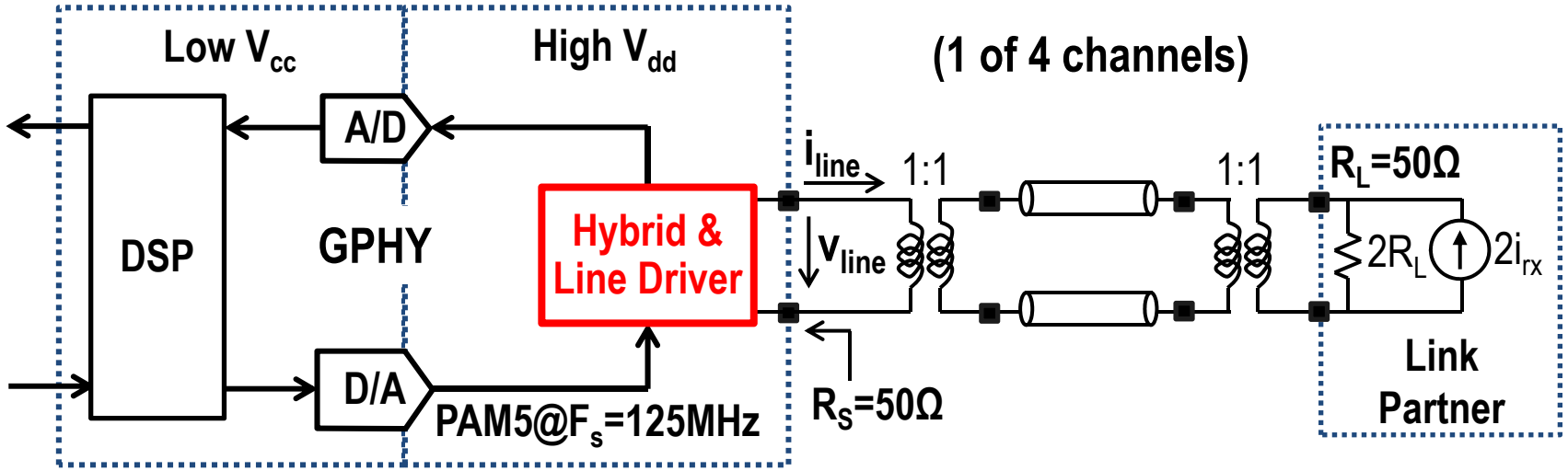
- Application Background: Gigabit Ethernet
- Full-Duplex (FD) Line Driver Architecture
- Current-Mode Class AB Output Stage
- Measurement Results and Summary

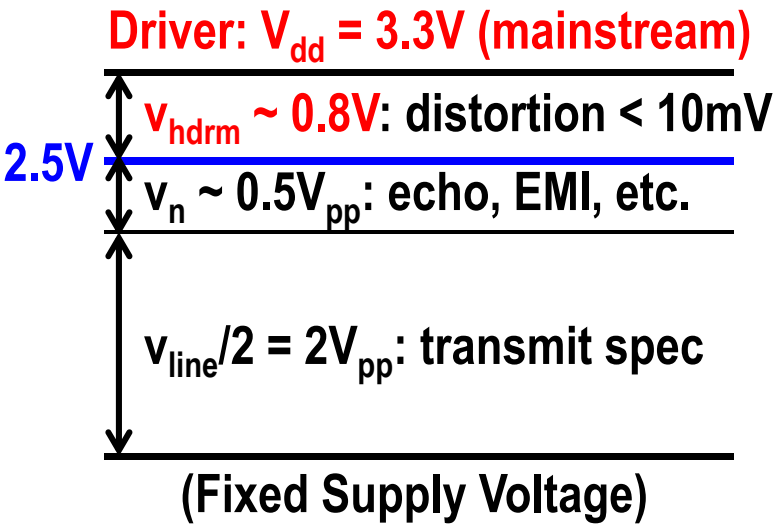
Reduce Gigabit Ethernet PHY (GPHY) Power



- IEEE 802.3ab 1000BASE-T dominates GPHY applications.
- GPHY power consumption has been reduced below 1W/port.
- Further power reduction is driven by ever-increasing throughput:
  - High Port Density: e.g., 16 or more ports/switch chip ➔ thermal cost
  - High Port Volume: >100M GPHY ports shipped/year ➔ energy cost

Eliminate GPHY Driver Voltage Headroom

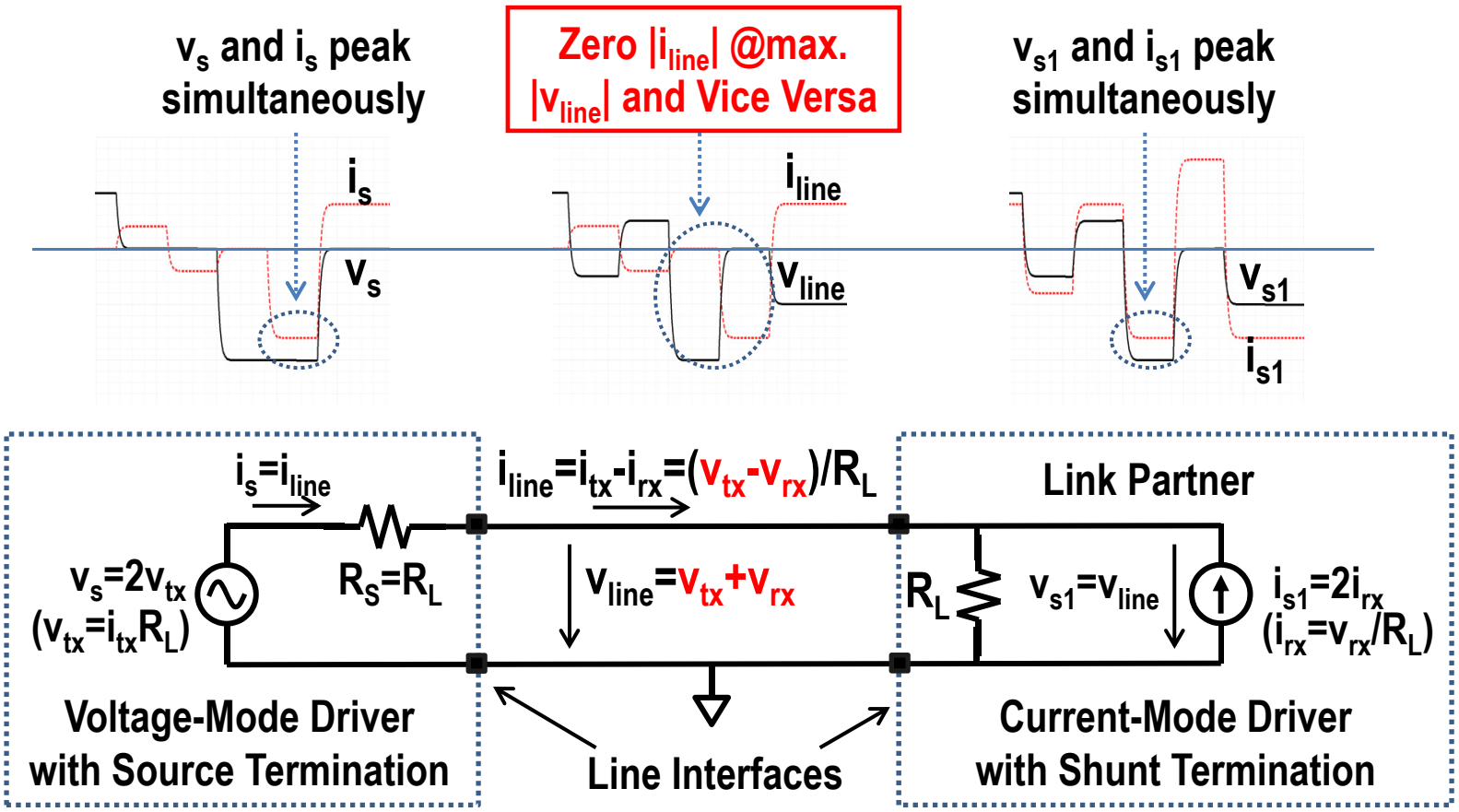




- GPHY power is dominated by the four drivers/port running at 3.3V.
- V_{dd} can be reduced by eliminating the headroom v_{hdrm} using the full-duplex driver running at 2.5V.

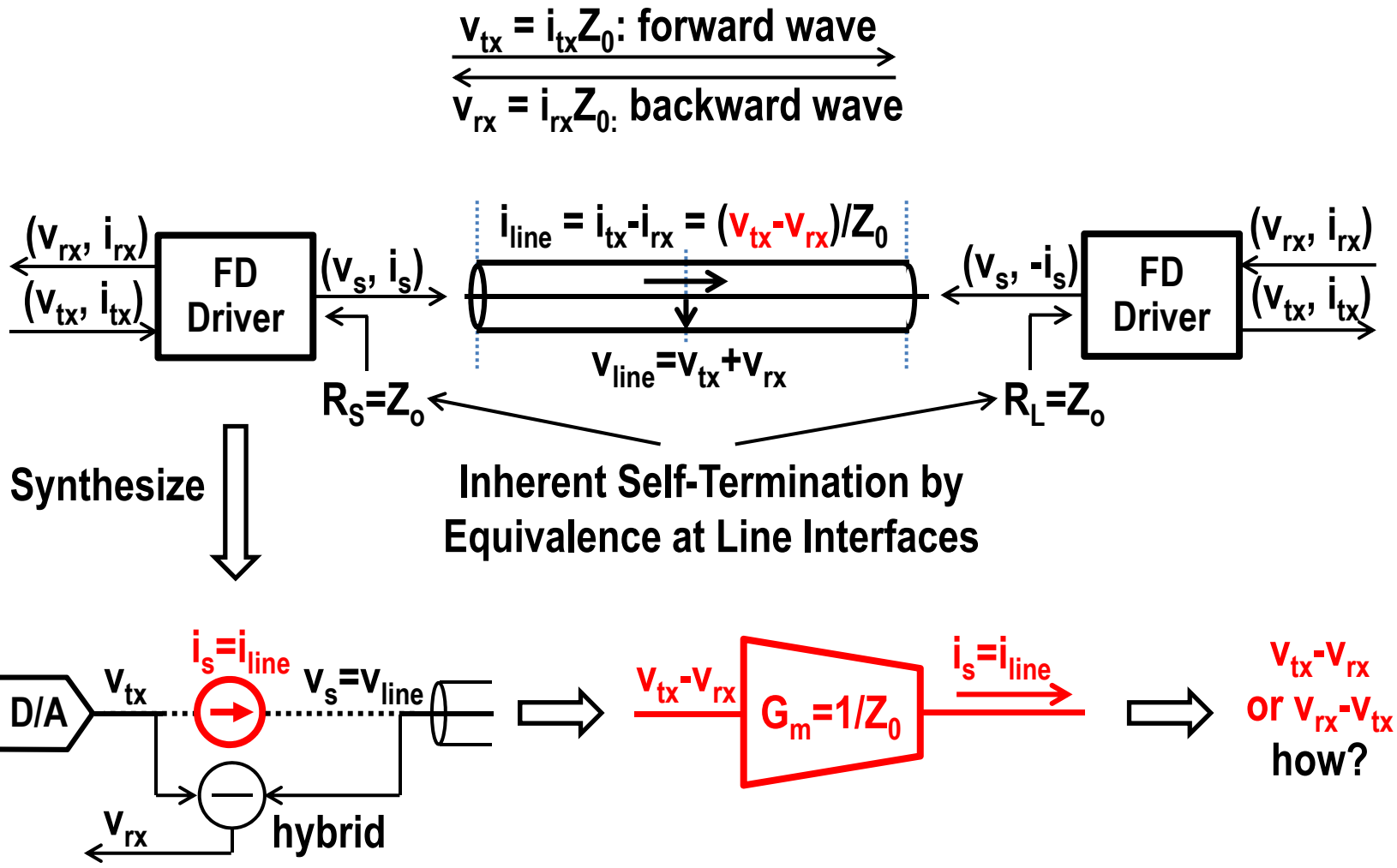
Derive the Rail-to-Rail Full-Duplex Driver Architecture

Conceive a Driver Directly Feeding the Line

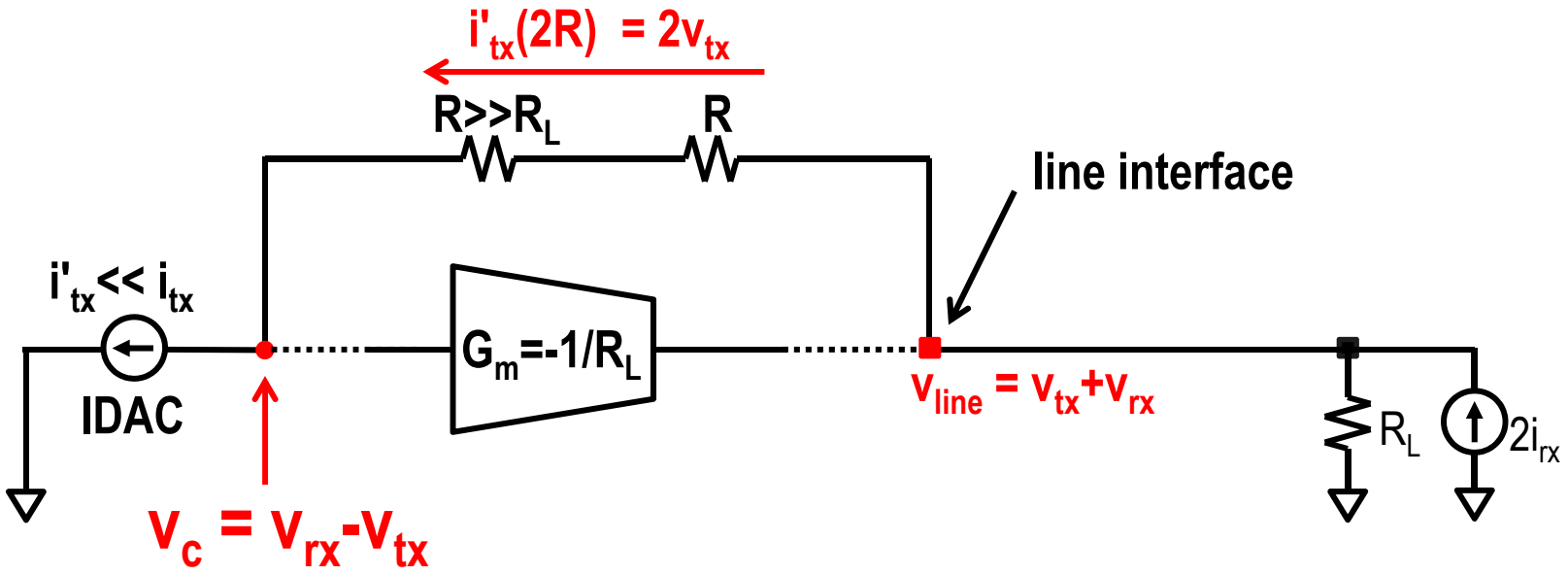


- If $v_s = v_{line}$, $i_s = i_{line}$ ➔ rail-to-rail possible: $v_{hdrm} = 0$

Synthesize the Driver by Interface Equivalence

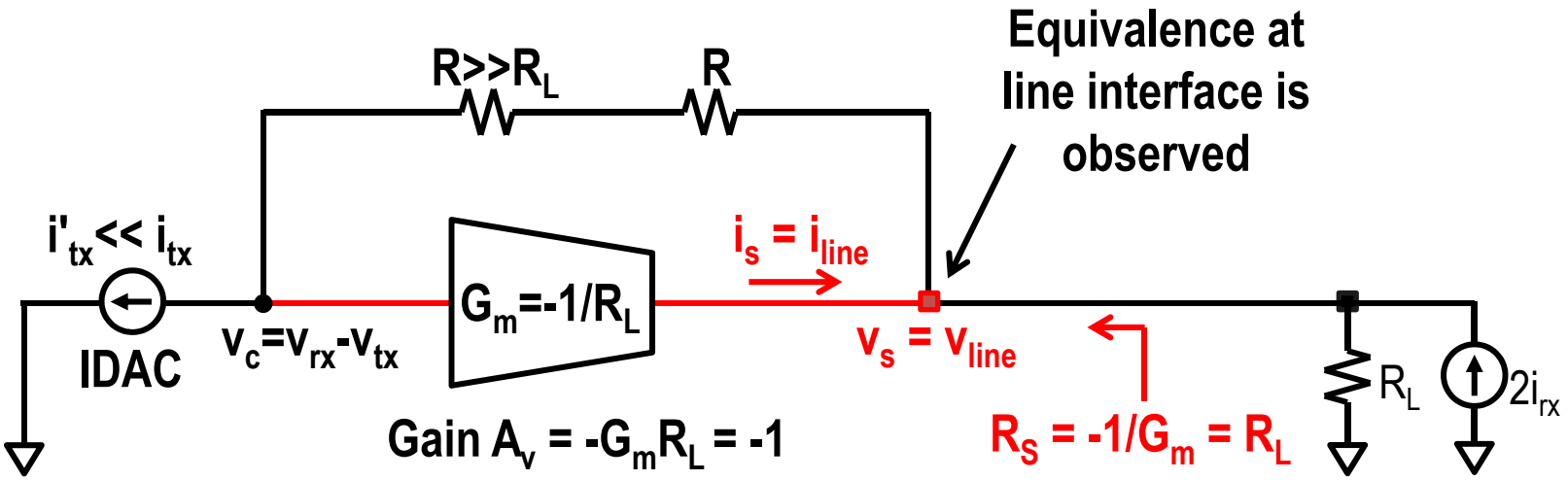


Generate $v_{rx} - v_{tx}$ as $v_{line} - 2v_{tx}$



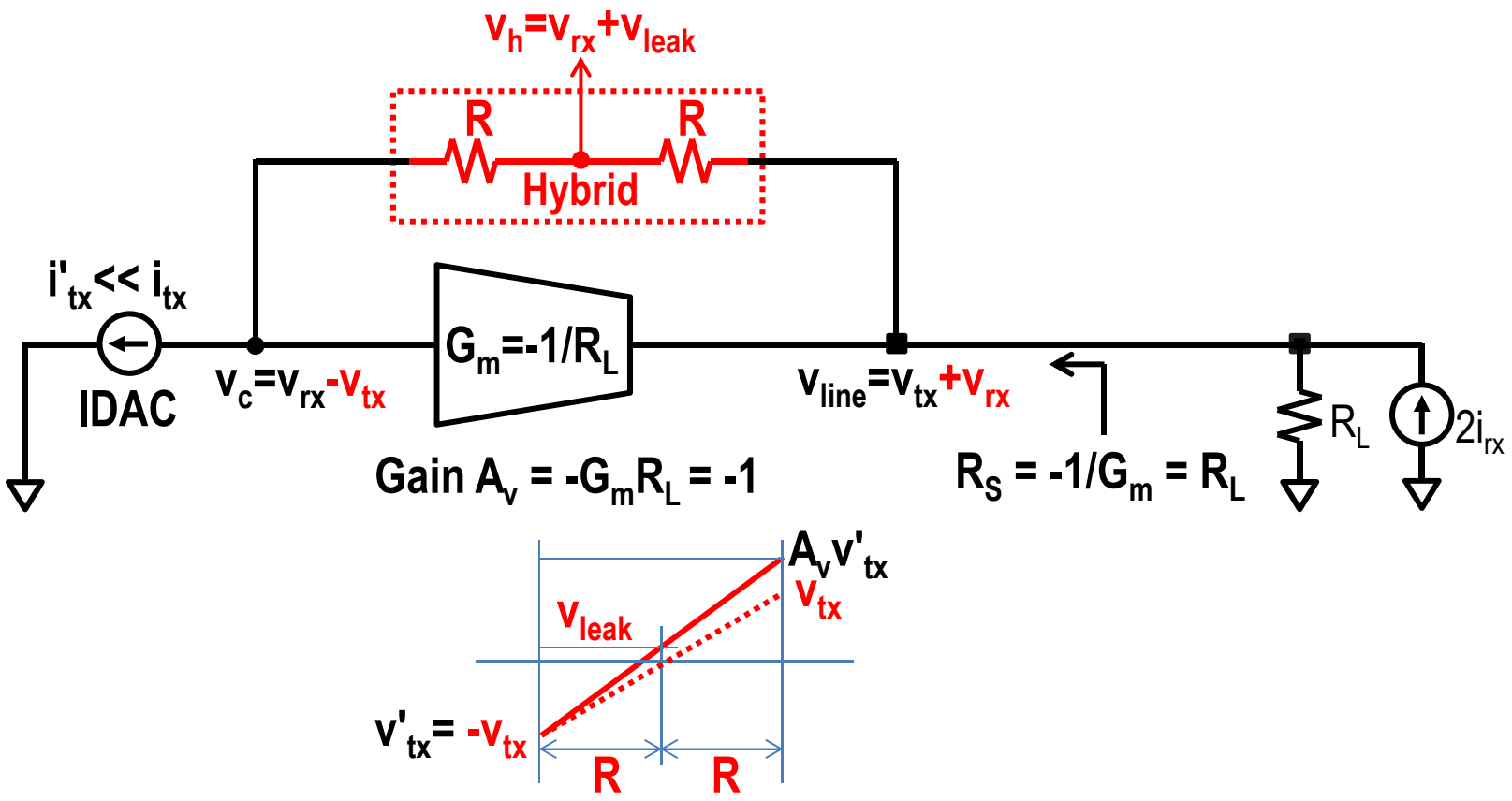
- Transmit current replica $i'_{tx} << i_{tx}$ is injected to the line interface with little perturbation to the line.

Connect $G_m = -1/R_L$ to Generate the Line Current



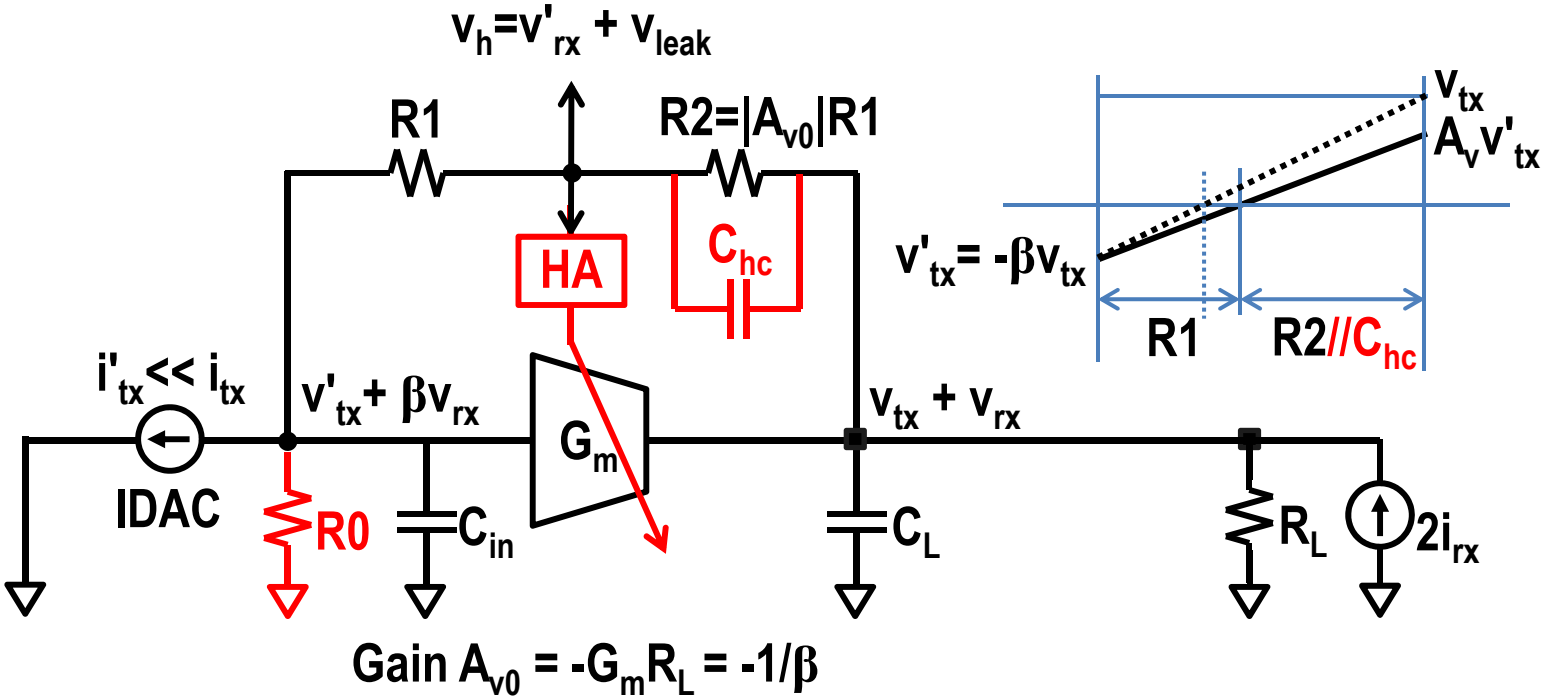
- $A_v = -1$ ➔ $R_s = R_L$: Inherently matched self-termination is confirmed

Extract Receive Signal v_{rx} at Feedback Midpoint



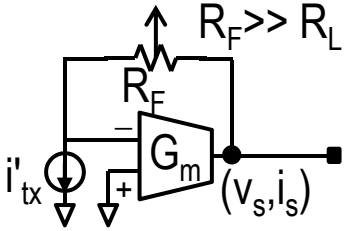
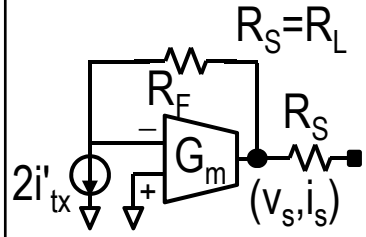
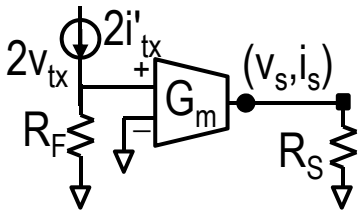
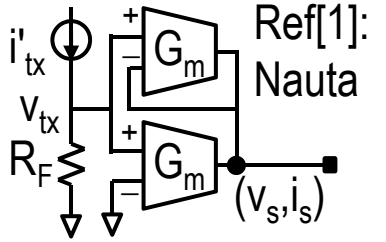
- $A_v = -1$, $R_s = R_L$, and $v_{leak} = 0$ simultaneously ➔ efficient adaptation

Refine the Full-Duplex Driver for Implementation



- R0 attenuates G_m input to avoid internal rail-to-rail swing.
- $C_{hc} = R_L C_L / R2$ compensates the gain roll-off effect on leakage.
- G_m is adapted against PVT/load variations by minimizing v_{leak}.

Ensure Power Efficiency for Full-Duplex Driver

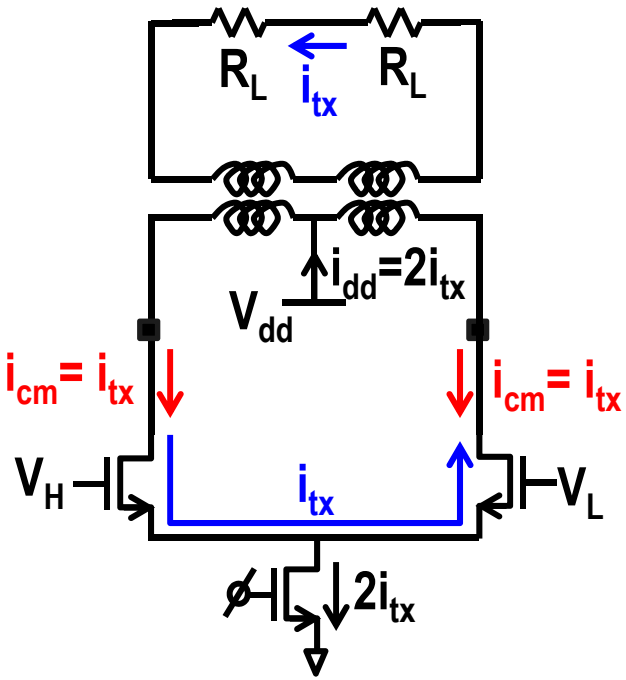
wideband drivers (shown single-endedly)	Full-Duplex, self termination	Voltage Mode, series termination	Current Mode, shunt termination	Current Mode, active termination
				
G_m	$1/R_L$	$>> 1/R_L$	$1/R_L$	$1/R_L$
output stage	class B (?) $i_{dd} \sim i_s$ (?)	class B $i_{dd} \sim i_s$	class A $i_{dd} > \max\|i_s\|$	class A $i_{dd} > \max\|i_s\|$
(i_s, v_s)	i_{line}, v_{line}	i_{line}, $2v_{tx}$	$2i_{tx}$, v_{line}	i_{line}, v_{line}
$2*\text{avg}(i_{dd})$	$\text{avg}\|i_{tx} - i_{rx}\|$	$\text{avg}\|i_{tx} - i_{rx}\|$	$2*\max\|i_{tx}\|$	$\max\|i_{tx}\| + \max\|i_{rx}\|$
$\min.V_{dd}$	$\max(v_{tx}+v_{rx})$	$\max(2v_{tx})+V_{hdrm}$	$\max(v_{tx}+v_{rx})+V_{hdrm}$	$\max(v_{tx}+v_{rx})+V_{hdrm}$

A current-efficient class B output stage must be used for the FD driver G_m.

Implement a Current Efficient Output Stage for the G_m

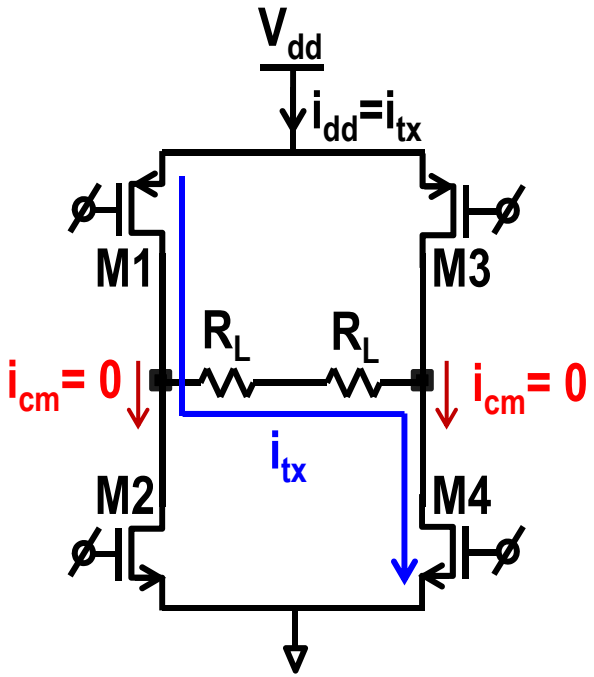
Choose Push-Pull Topology for G_m Output Stage

class B current steering (CML)



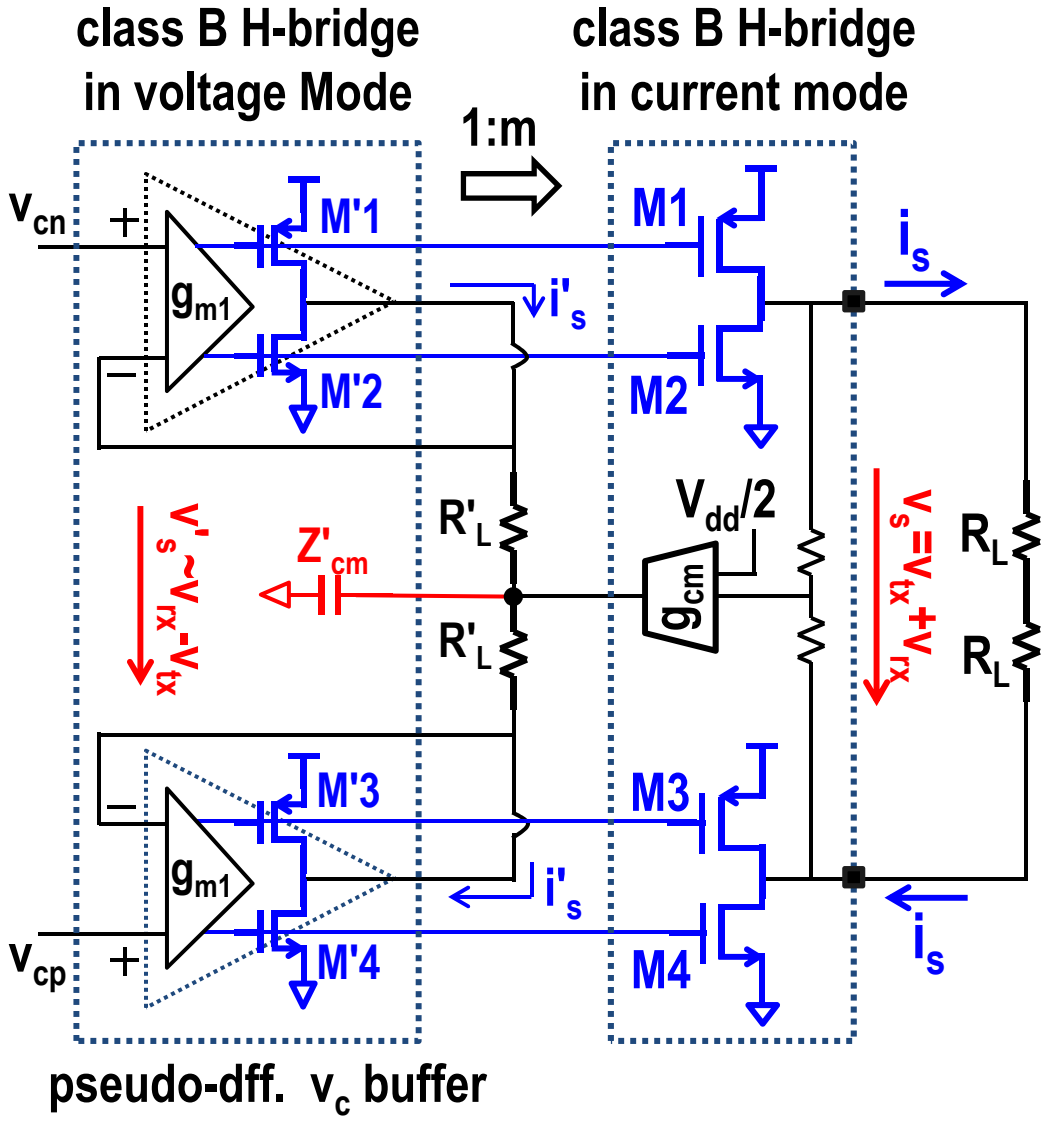
- x 50% Current efficiency
- x EM interference (EMI)
- x Usually operate in class A

class B push-pull (H-Bridge)



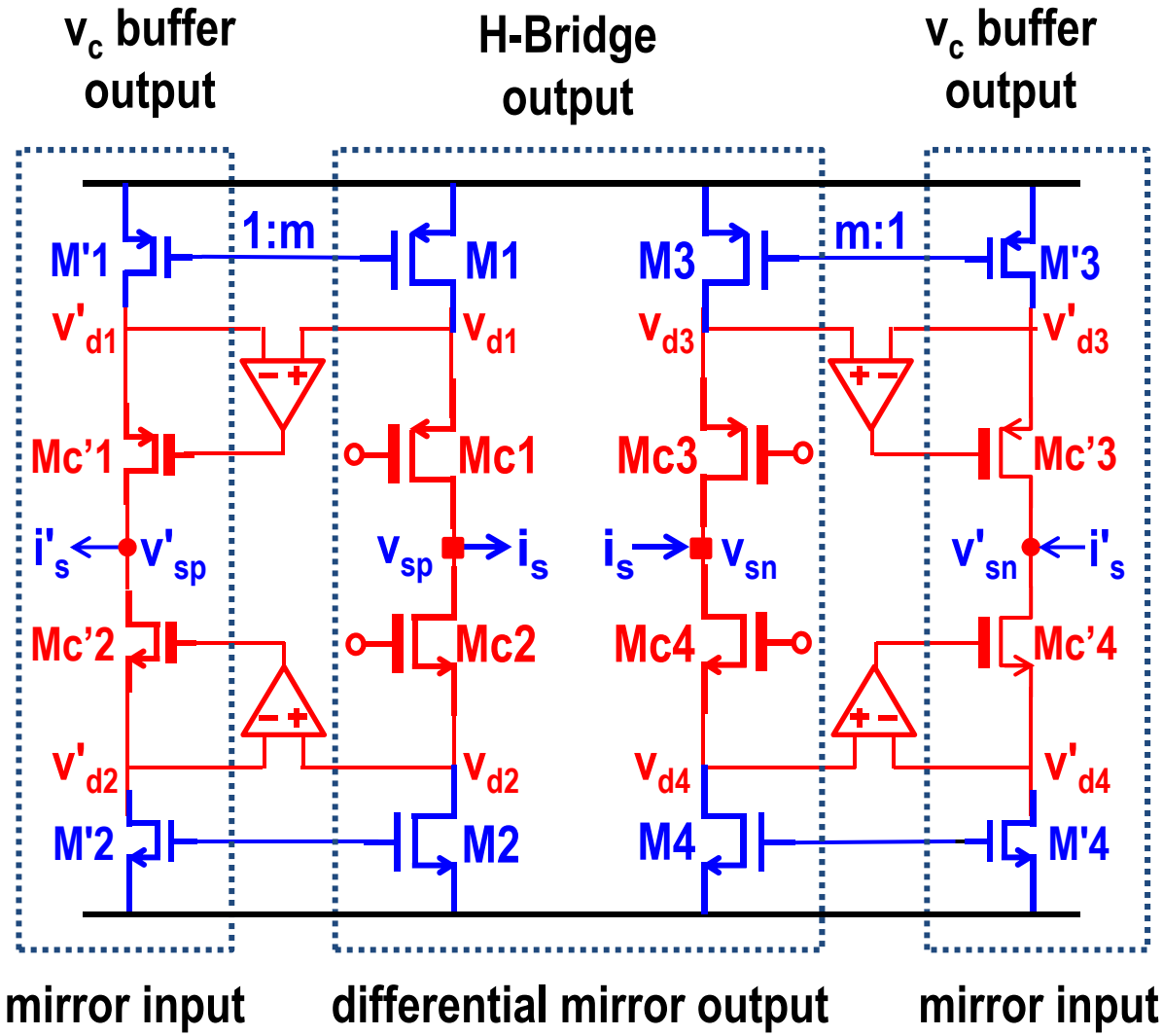
- ✓ 100% Current efficiency
- x Inherently nonlinear
- x Need to set CM voltage

Solve the H-Bridge Linearity and CM Issues



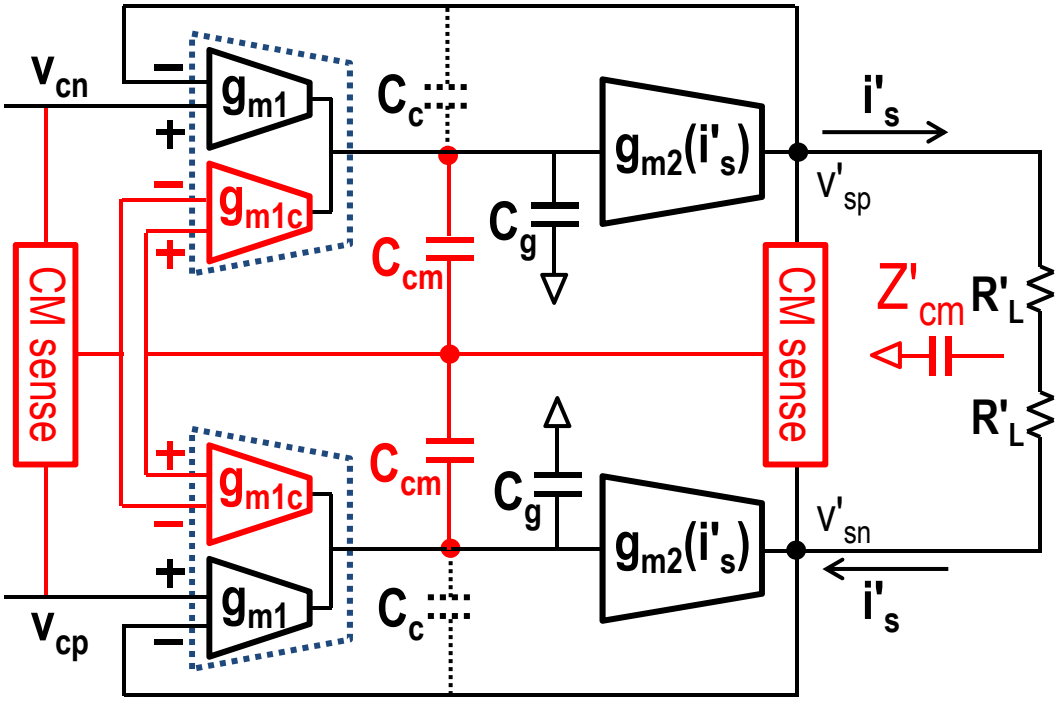
- $i_s = mi'_s$ ($m >> 1$)
- $G_m(DM) = m/(2R'_L)$
- g_{cm} loop sets CM
- x Mismatch: $v_s \neq v'_s$
- x $G_m(CM) = m/Z'_{cm}$,
  Z'_{cm}: AC ground

Boost Output Linearity for Rail-to-Rail Operation



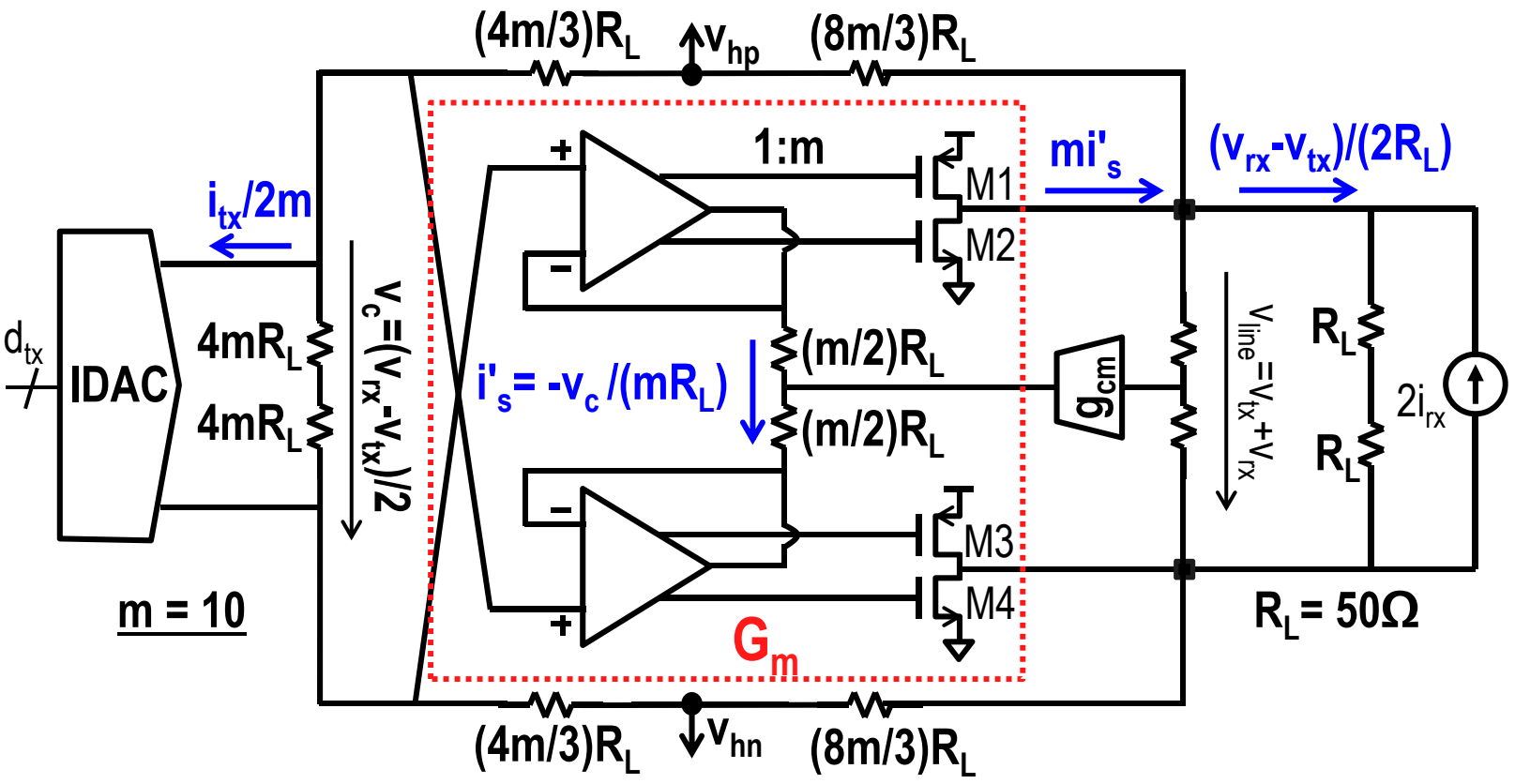
- Drain voltages v_{d1-4} vary with the signal at rail-to-rail output swing.
- Op-amp loops force v'_{d1-4} to track v_{d1-4}.
- Small op-amp overhead for m >> 1

Disconnect Z'_{cm} and Compensate the CM Loop



- The buffer becomes differential with the center tap Z'_{cm} removed.
- The resulted CM loop needs more compensation than the DM loop.
- C_{cm} and g_{m1c} compensate the CM loop while preserving DM BW.

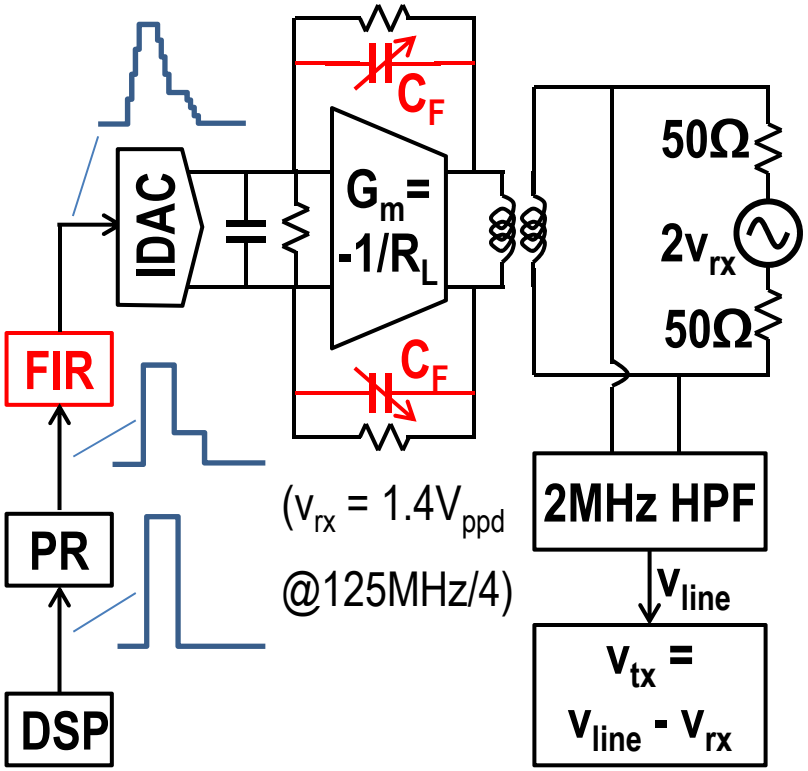
Finalize the Differential Full-Duplex Driver

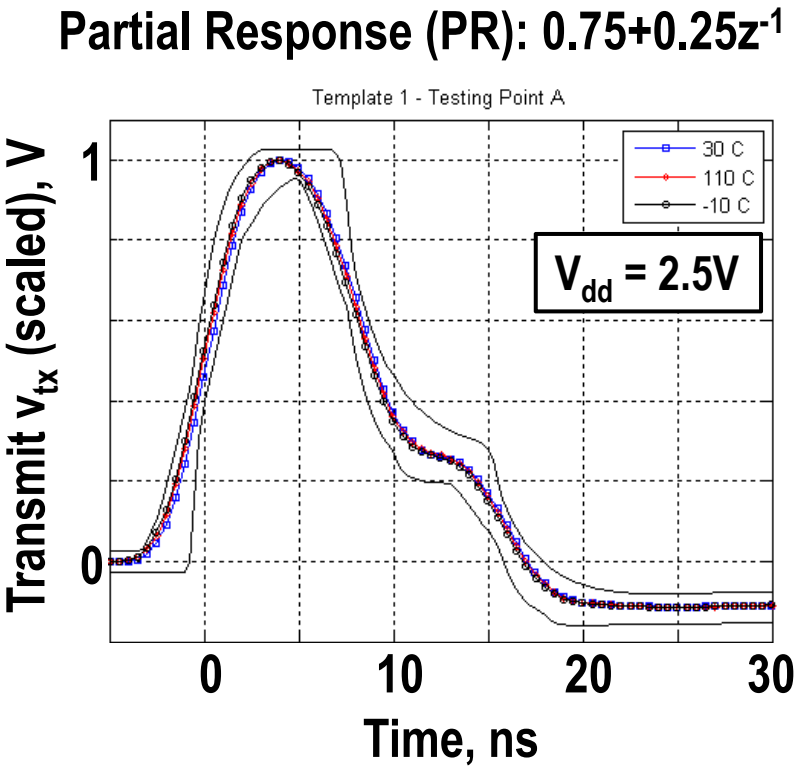


- Current steering IDAC output voltage is halved for headroom.
- Voltage gain doubled: $A_v = -2$ with $G_m(DM) = -1/R_L$ and $v_h = 2v_{rx}/3$.
- Active output CM termination impedance = $1/(mg_{cm}) \geq R_L/2$.

IEEE 802.3ab Compliance Test Results and Summary

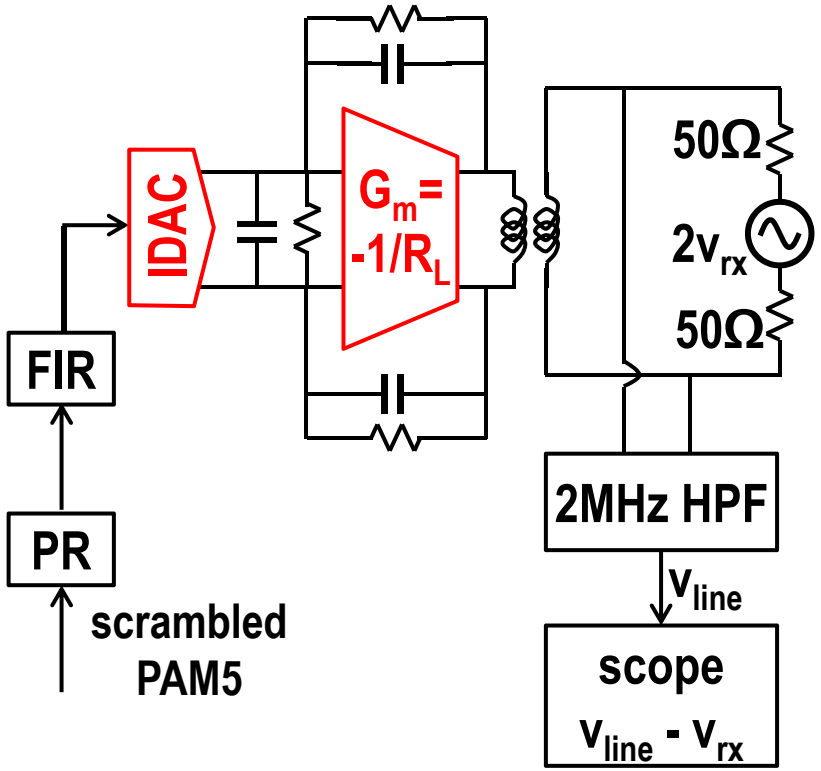
1000BASE-T Template Test

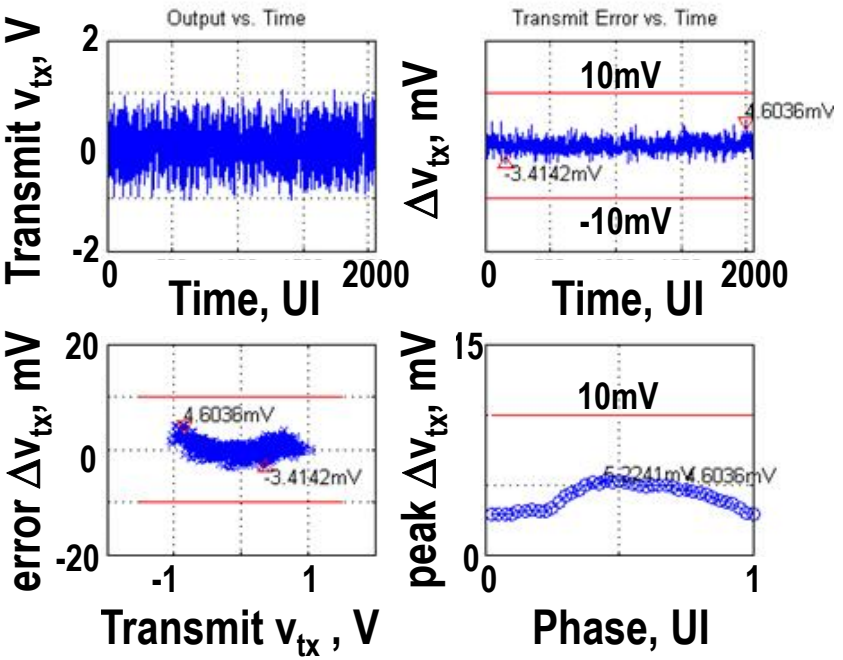




- Driver output pulse responses measured at V_{dd} = 2.5V all fit the templates, insensitive to temperature variation.

1000BASE-T Distortion Measurement

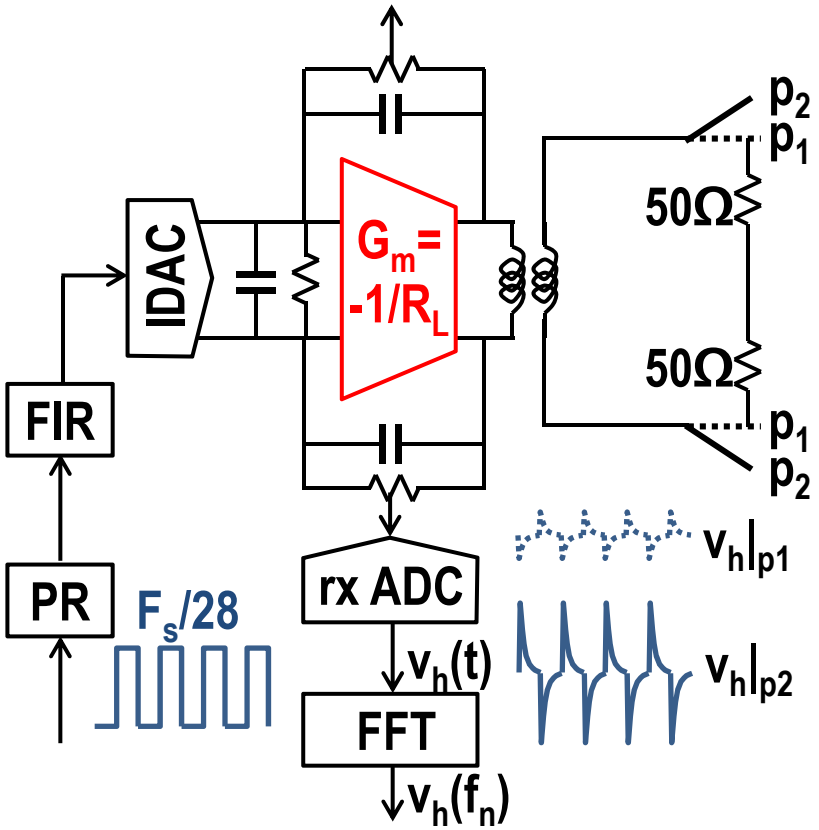


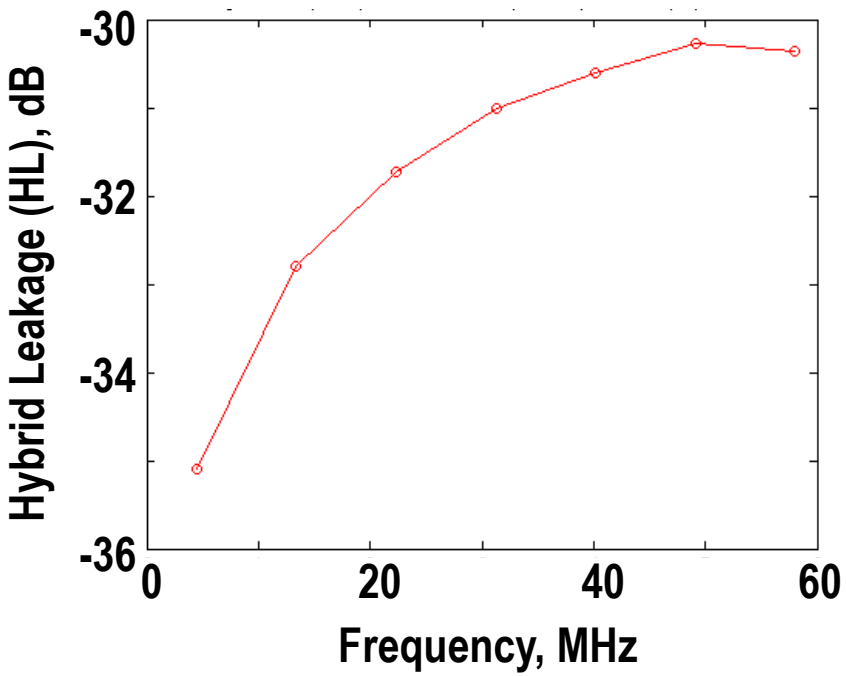


(V_{dd} = **2.5V**, Temp = 110°C,
v_{rx} = 2.7V_{ppd} @125MHz/6)

- Distortion or transmit waveform deviation from the best fit is measured smaller than the 10mV spec at 2.5V and 110°C.

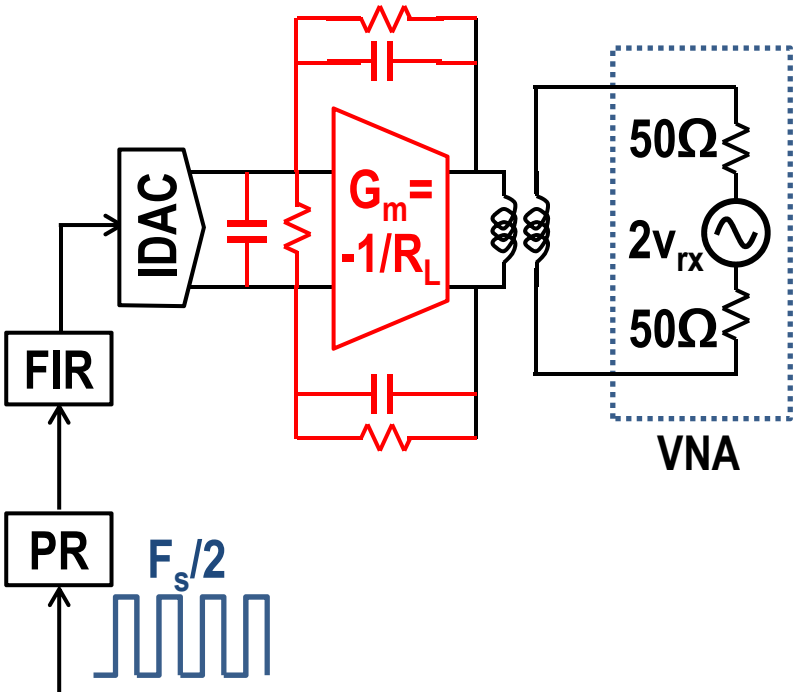
Hybrid Leakage Measurement

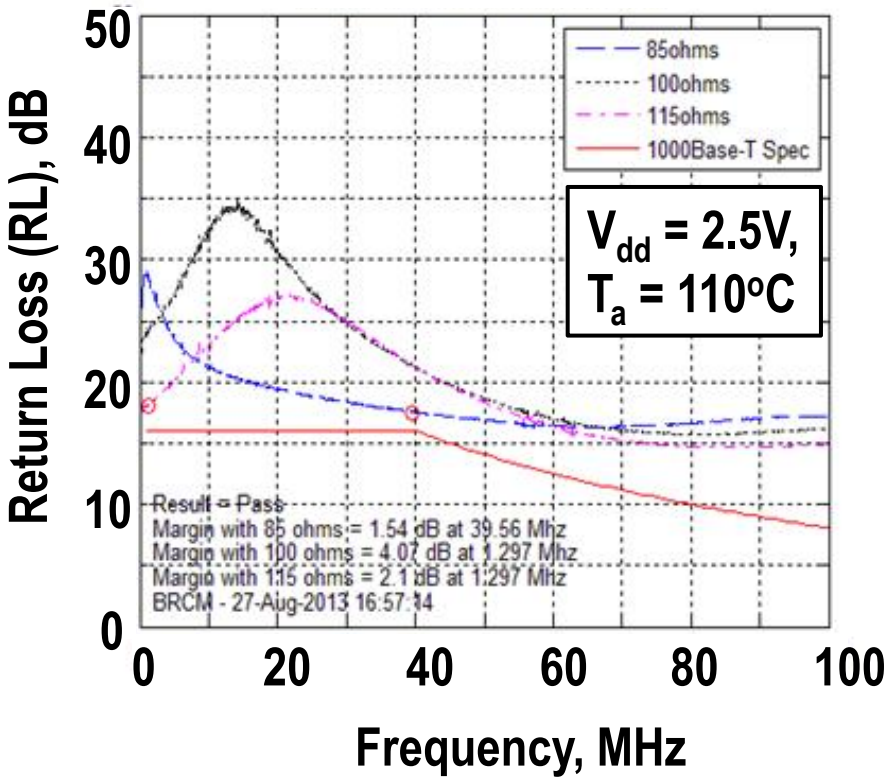




- Hybrid Leakage ≡ $20*\log(v_{leak(pp)}/v_{h(pp)}|_{Vrx=Vtx}) = v_h(f_n)|_{p1}(dB) - v_h(f_n)|_{p2}(dB)$.
- $v_h|_{p1}$ and $v_h|_{p2}$ are measured with zero and total reflection, respectively.
- Hybrid leakage is measured lower than -30dB at frequencies up to 60MHz.

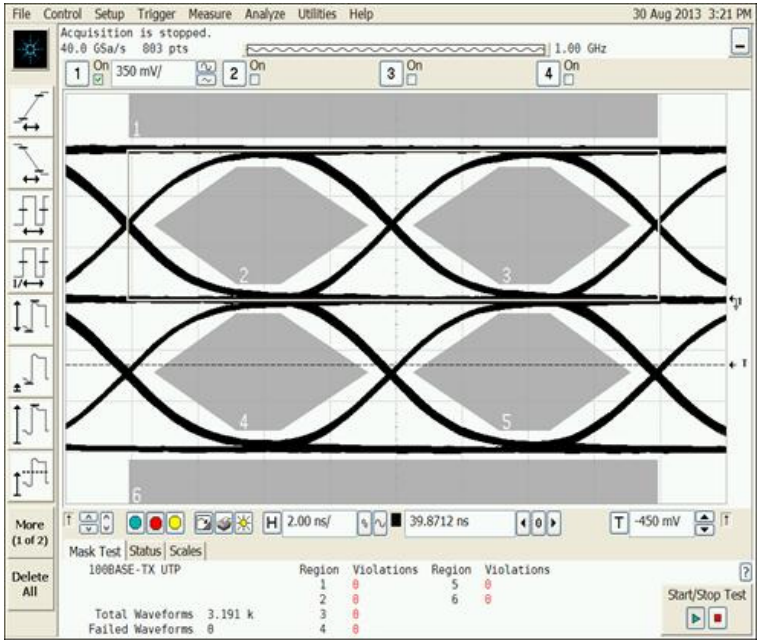
Return Loss (RL) Measurement

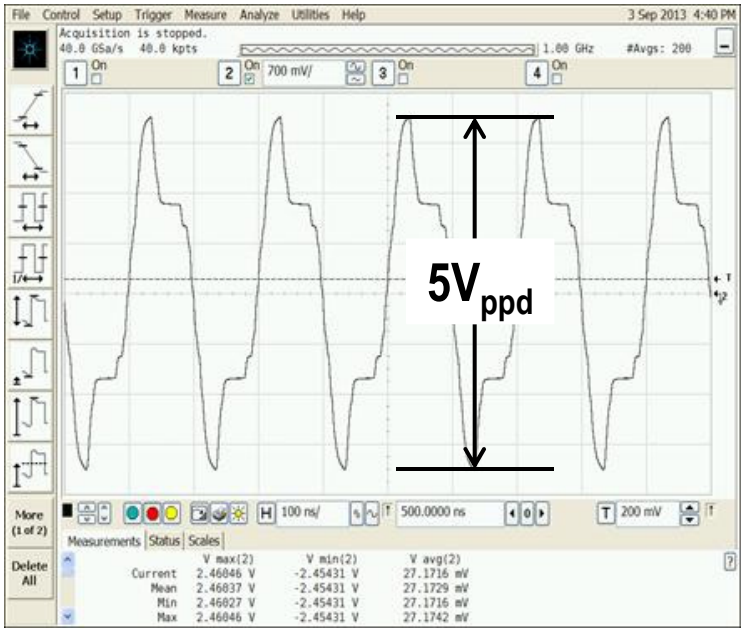




- Return loss curves measured at V_{dd} = 2.5V with Z_o = 100±15Ω are all above the return loss mask.

100BASE-TX/10BASE-T Measurements





100Tx AOI eye diagram, V_{dd} = 2.5V, 30°C

10BT 1010 pattern, V_{dd} = 3V, 30°C

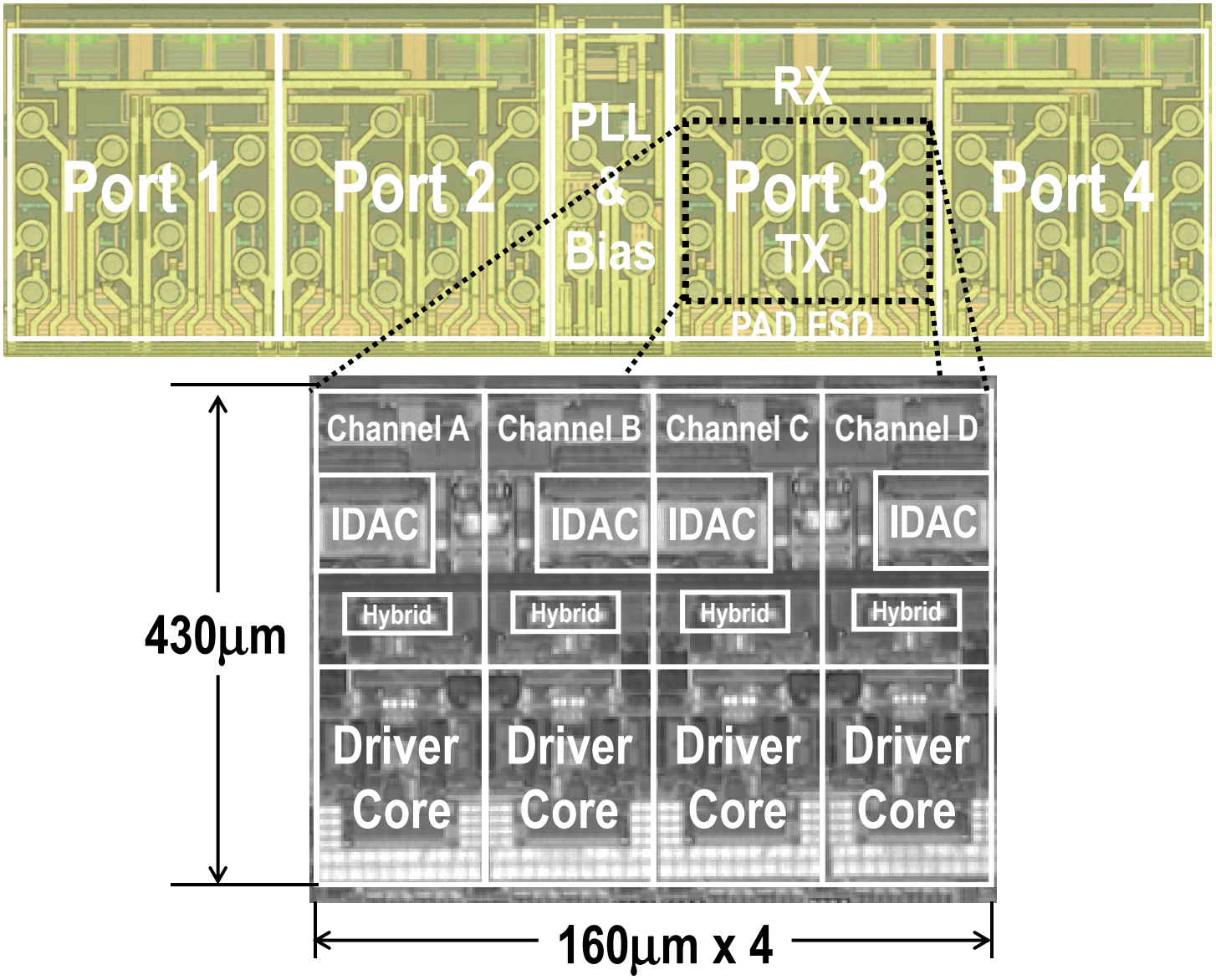
- A single full-duplex driver supports all three Ethernet modes (1000/100/10 BASE-T) with a 3.3V supply.

Advance the State of the Arts

	This full-duplex driver		Ref [5]: Stiurca, *ISCAS* 2005	Ref [4]: Babanezhad, *JSSC* 1999
Compliance	1000/100/10BT	1000/100BT	1000/100BT	100/10BT
Supply	3.3V	2.5V	3.3V	3.3V
Technology	28nm CMOS + 1.8V option		0.13μm CMOS	0.4μm CMOS
Operation	class AB current mode		voltage mode	voltage mode
Transformer	1:1		1:1	1:2
Area	160x430μm^2 = 0.069mm^2		0.06mm^2	0.15mm^2
Idle Current	5.6mA		8mA	7.6mA

- 2.5V GPHY driver saving >24% power from the 3.3V mainstream.
- Compliance with all three Ethernet modes with a 3.3V supply.

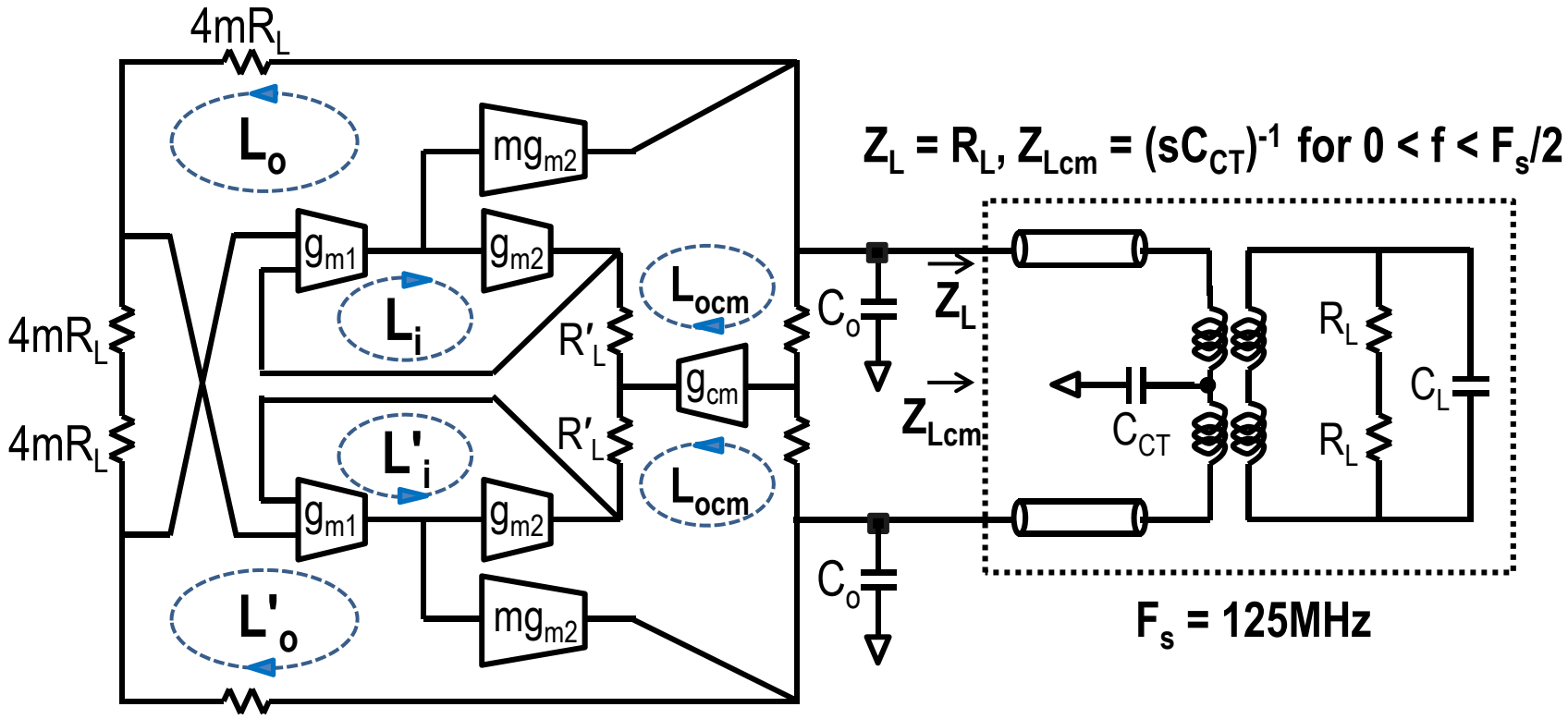
A Quad-Port GPHY AFE Micrograph



SUMMARY

- Derived a rail-to-rail full-duplex driver architecture based on equivalence at the line interface.
- Implemented a class-AB push-pull output stage operating in current mode for current efficiency.
- Achieved a 2.5V GPHY driver saving 24% in power dissipation from the mainstream 3.3V drivers.

Optimize Multi-Loop Performance and Stability



- Outer loop (L_o, L'_o, L_{ocm}) BW ~ 200MHz > $F_s/2$ for performance.
- BW << Inner loop (L_i, L'_i) unity gain freq. GBW ~ 1GHz for stability.
- Load is dominated by parasitics and transmission line effect at GBW.

A 4-to-10.5Gb/s 2.2mW/Gb/s Continuous-Rate Digital CDR with Automatic Frequency Acquisition in 65nm CMOS

Guanghua Shu[1], Woo-Seok Choi[1], Saurabh Saxena[1], Tejasvi Anand[1], Amr Elshazly[2], and Pavan Kumar Hanumolu[1]

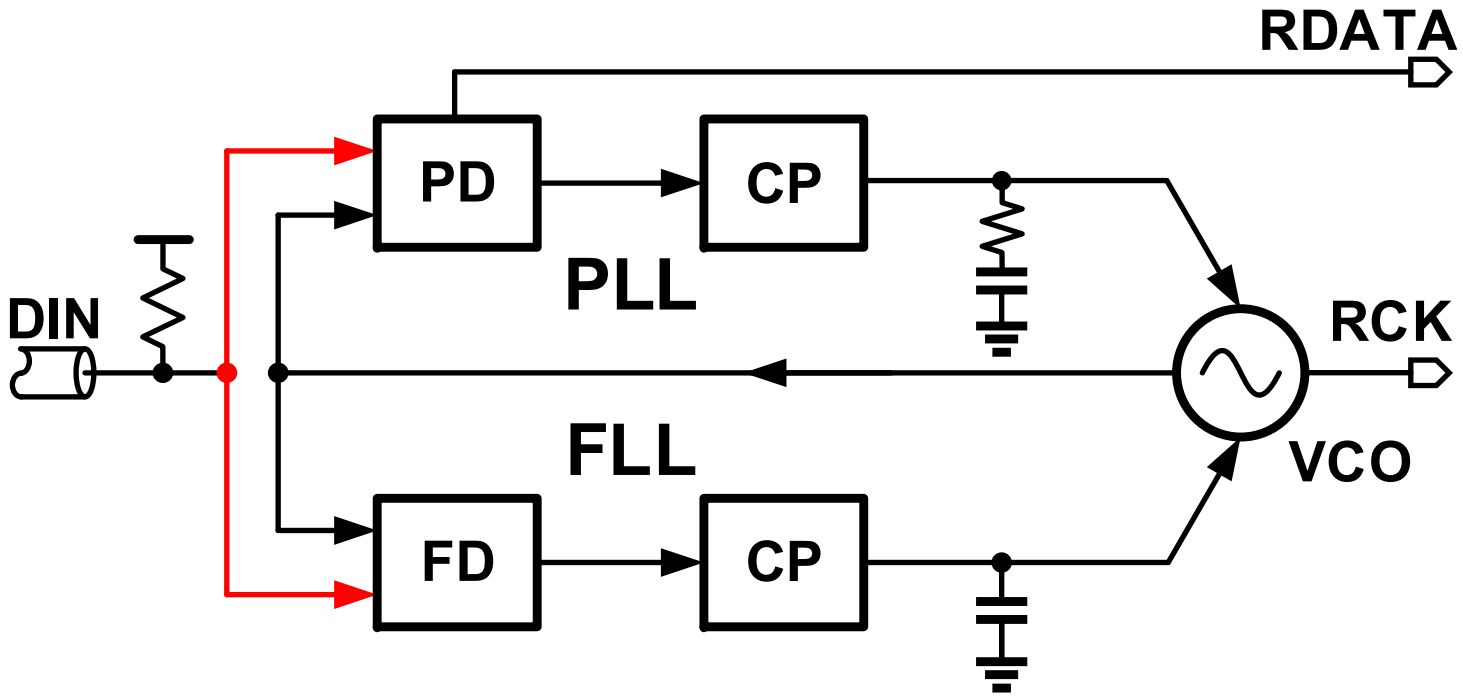
[1] University of Illinois at Urbana-Champaign, IL, USA

[2] Intel, Hillsboro, OR, USA

Outline

- **Introduction**
- **Automatic Frequency Acquisition**
- **CDR Architecture**
- **Measurement Results**
- **Summary**

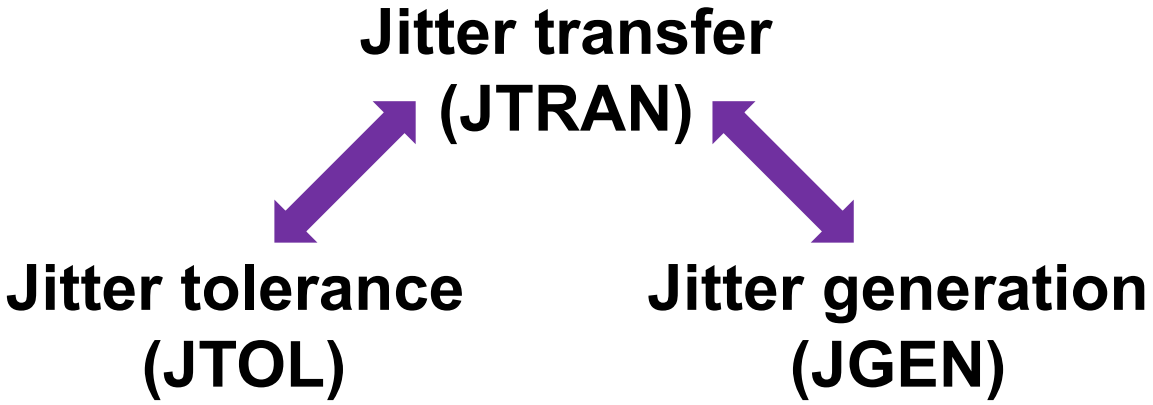
Continuous-Rate CDR



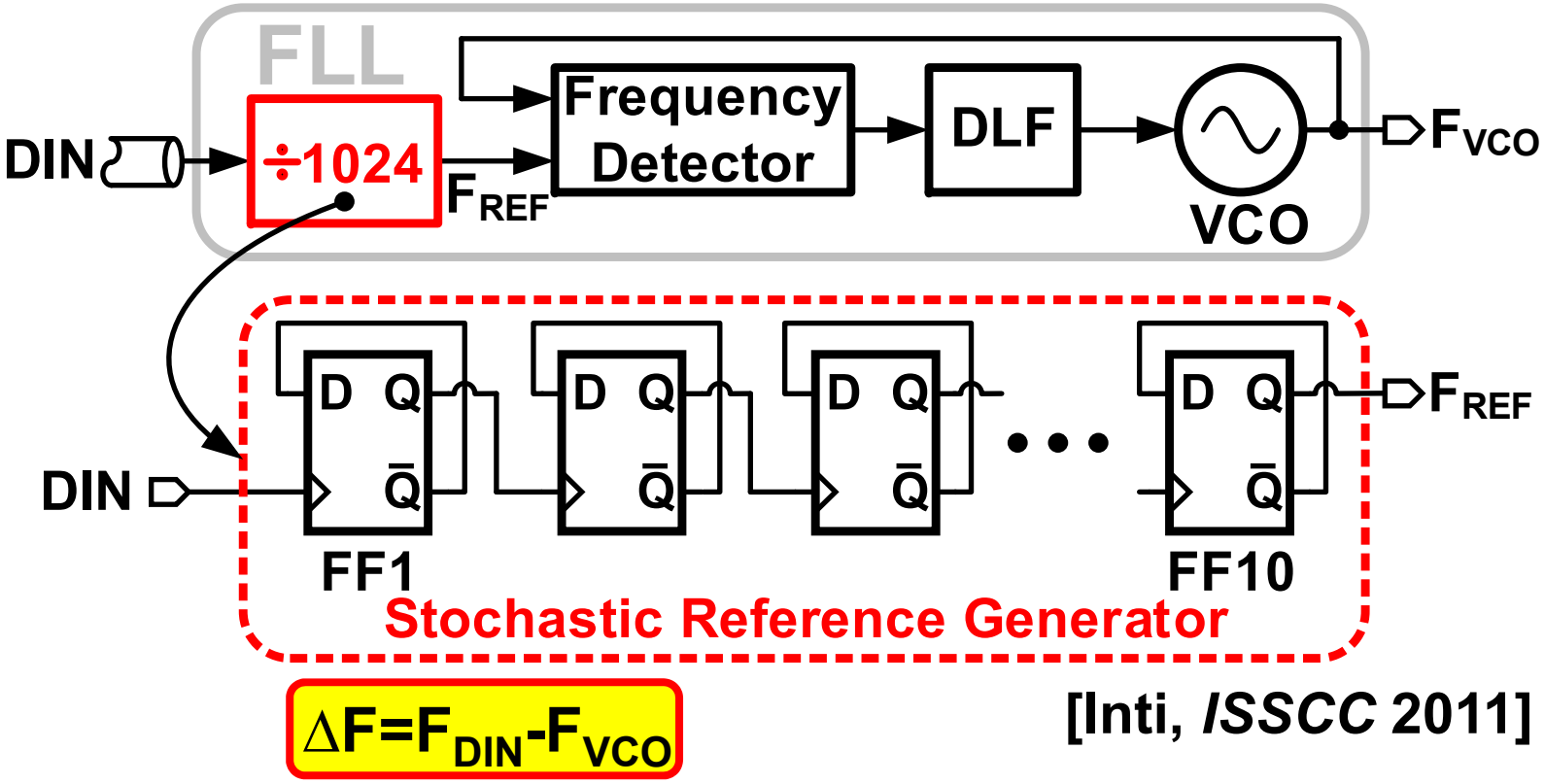
- Both optical and electrical communication systems
- Operation over wide data rate range
- Single-chip multi-standard solution

CDR Design Challenges

- Automatic frequency acquisition
- JTRAN/JTOL/JGEN tradeoffs



Freq. Acquisition w/ Stochastic Divider

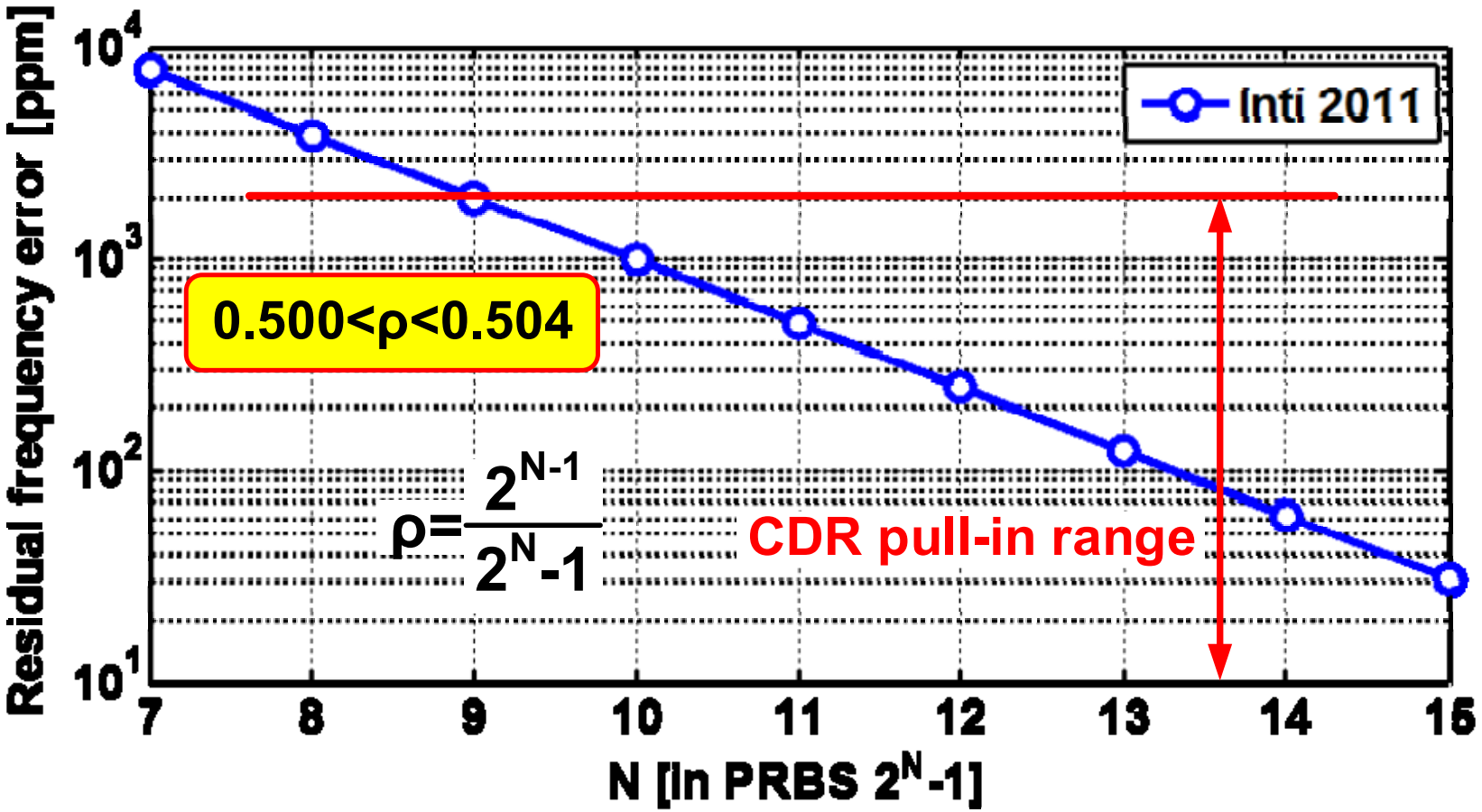


✓ **Divide DIN to extract stochastic reference F_{REF}**

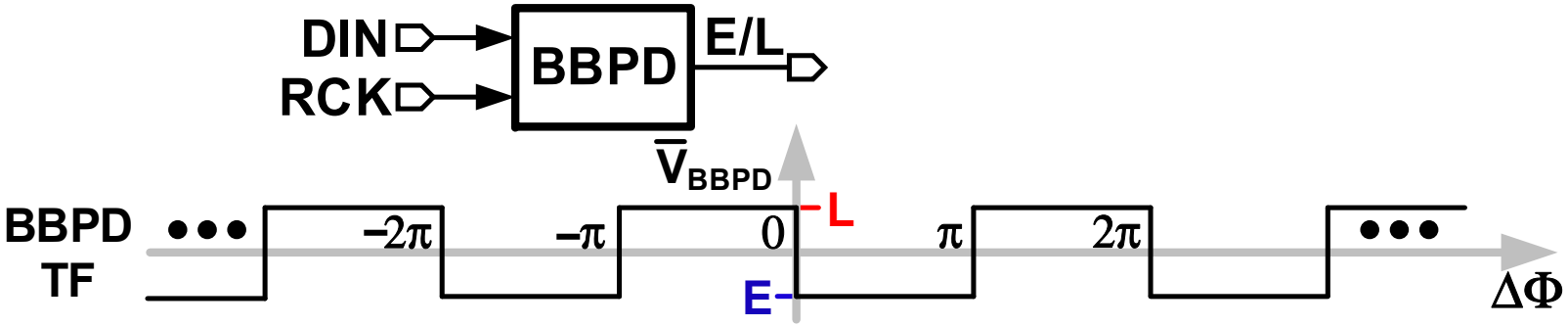
× **Frequency error ΔF depends on transition density ρ**

Transition Density Dependence

- Residual frequency error $\Delta F=2x(\rho-0.5)x10^6$ [ppm]

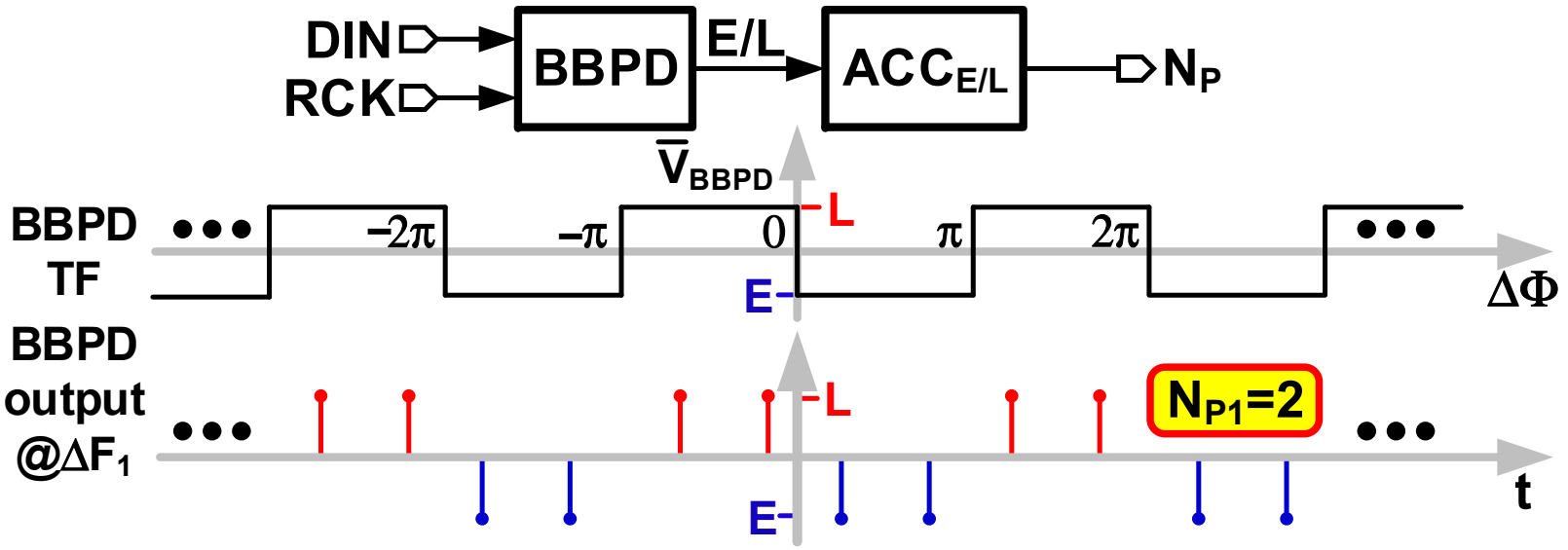


Principle of Frequency Detection



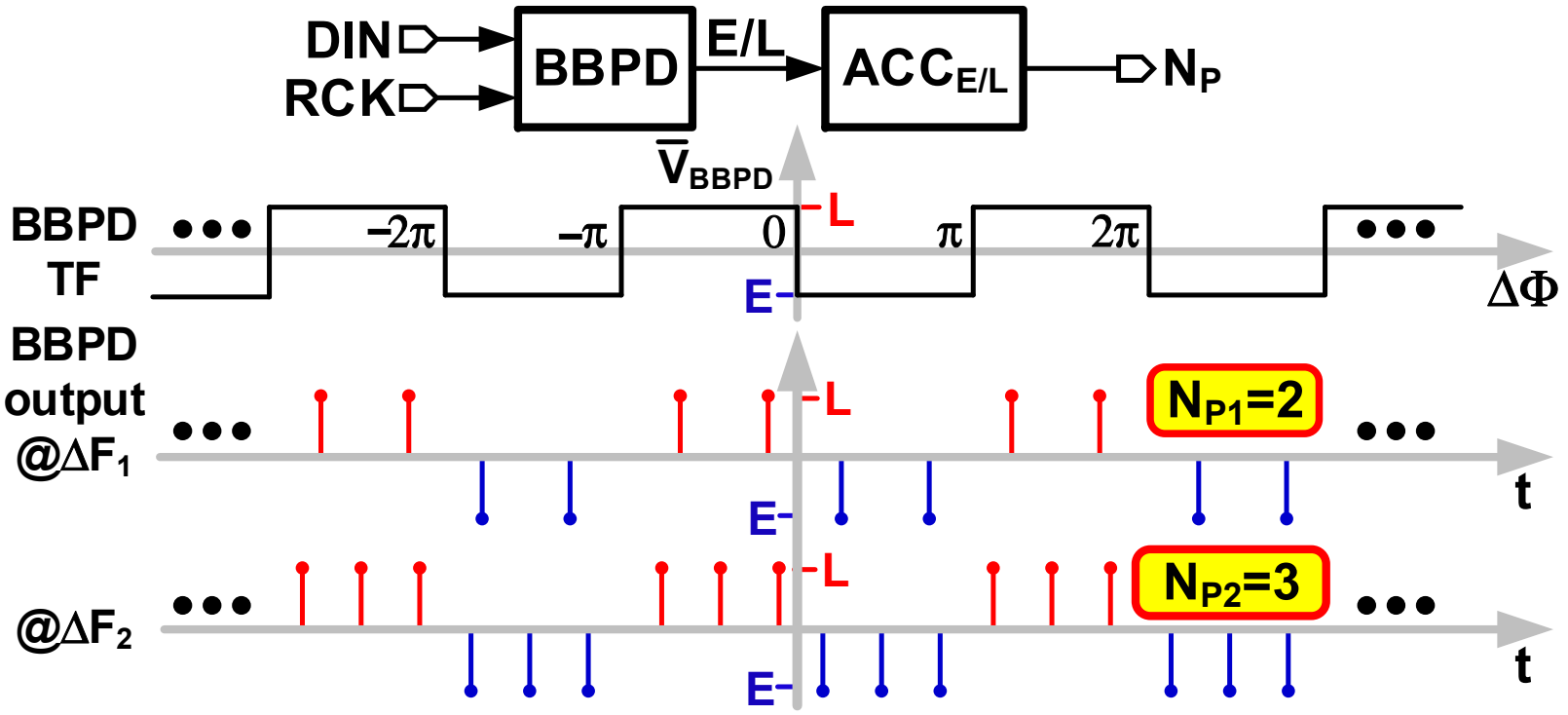
- BBPD output changes sign at $\Delta\Phi = n\pi$

Principle of Frequency Detection



N$_P$ is consecutive Early or Late number in π interval of ΔΦ

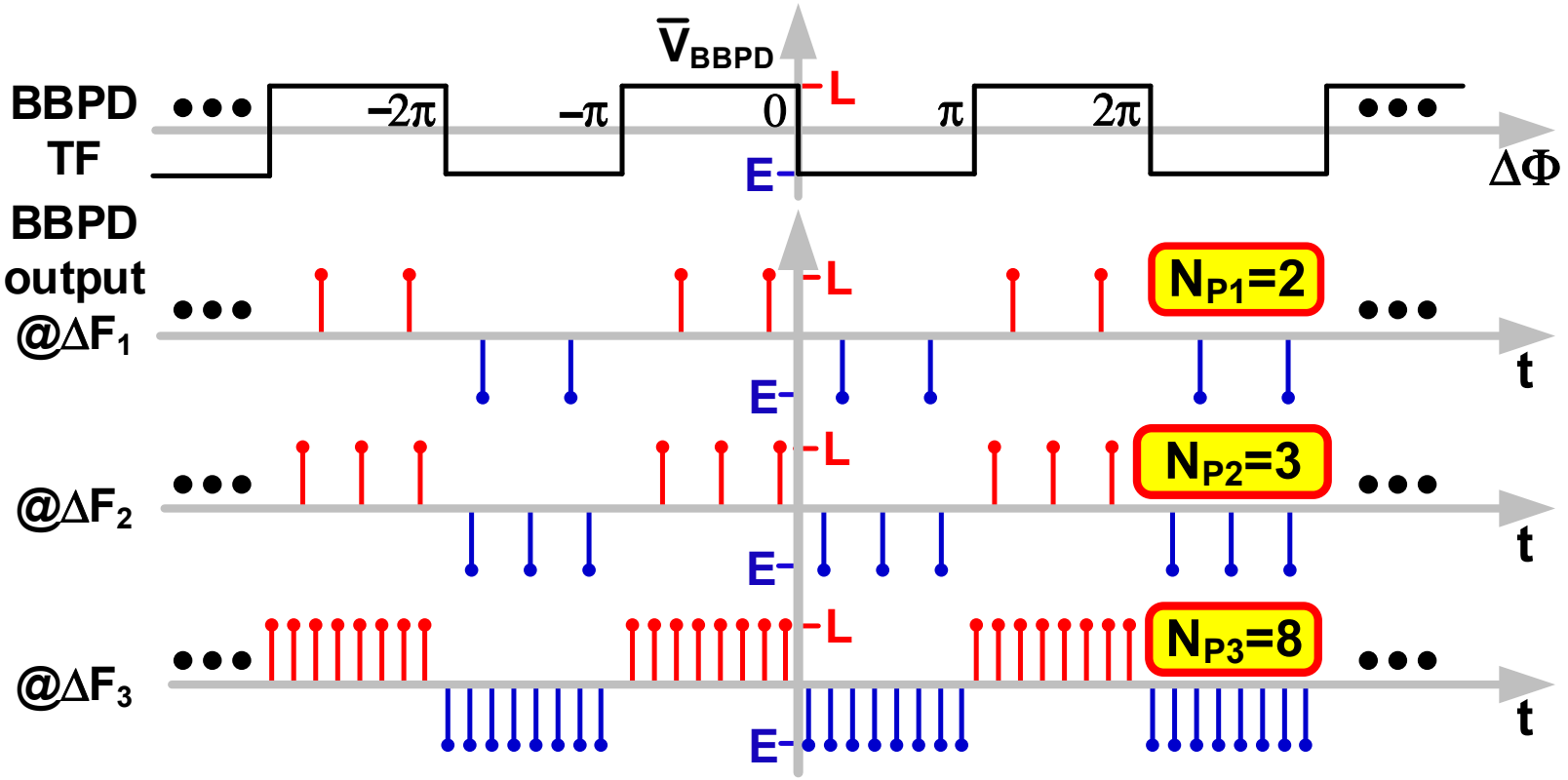
Principle of Frequency Detection



$\Delta F_2 < \Delta F_1$ leads to $N_{P2} > N_{P1}$

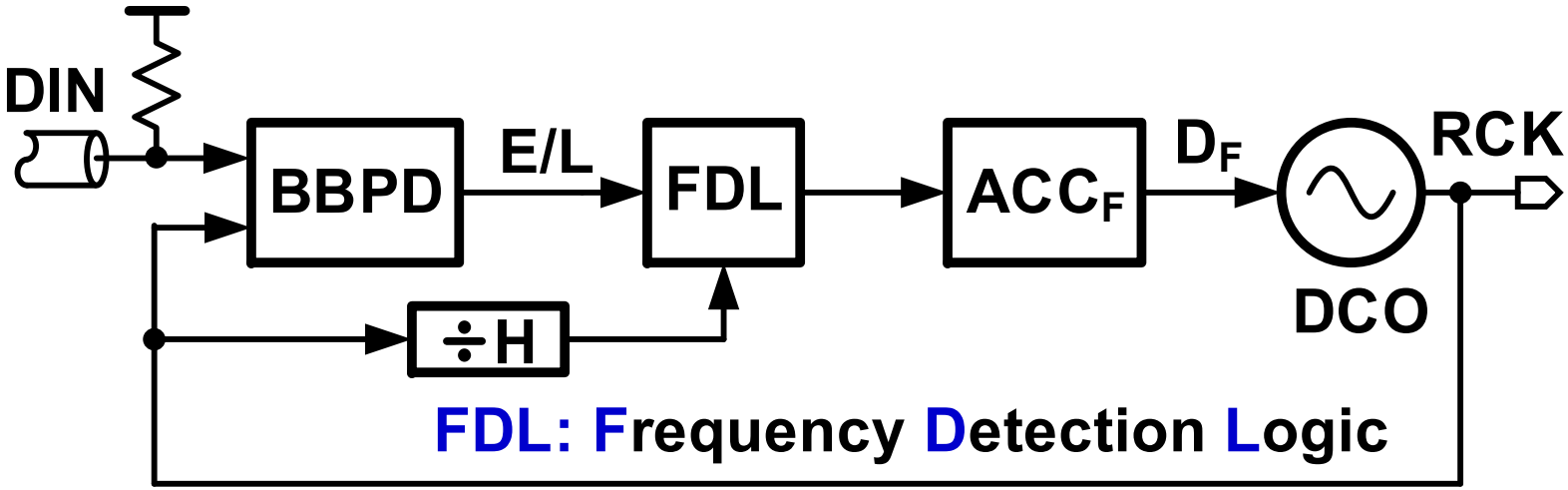
Principle of Frequency Detection

$\Delta F_3 < \Delta F_2 < \Delta F_1 \rightarrow N_{P3} > N_{P2} > N_{P1}$



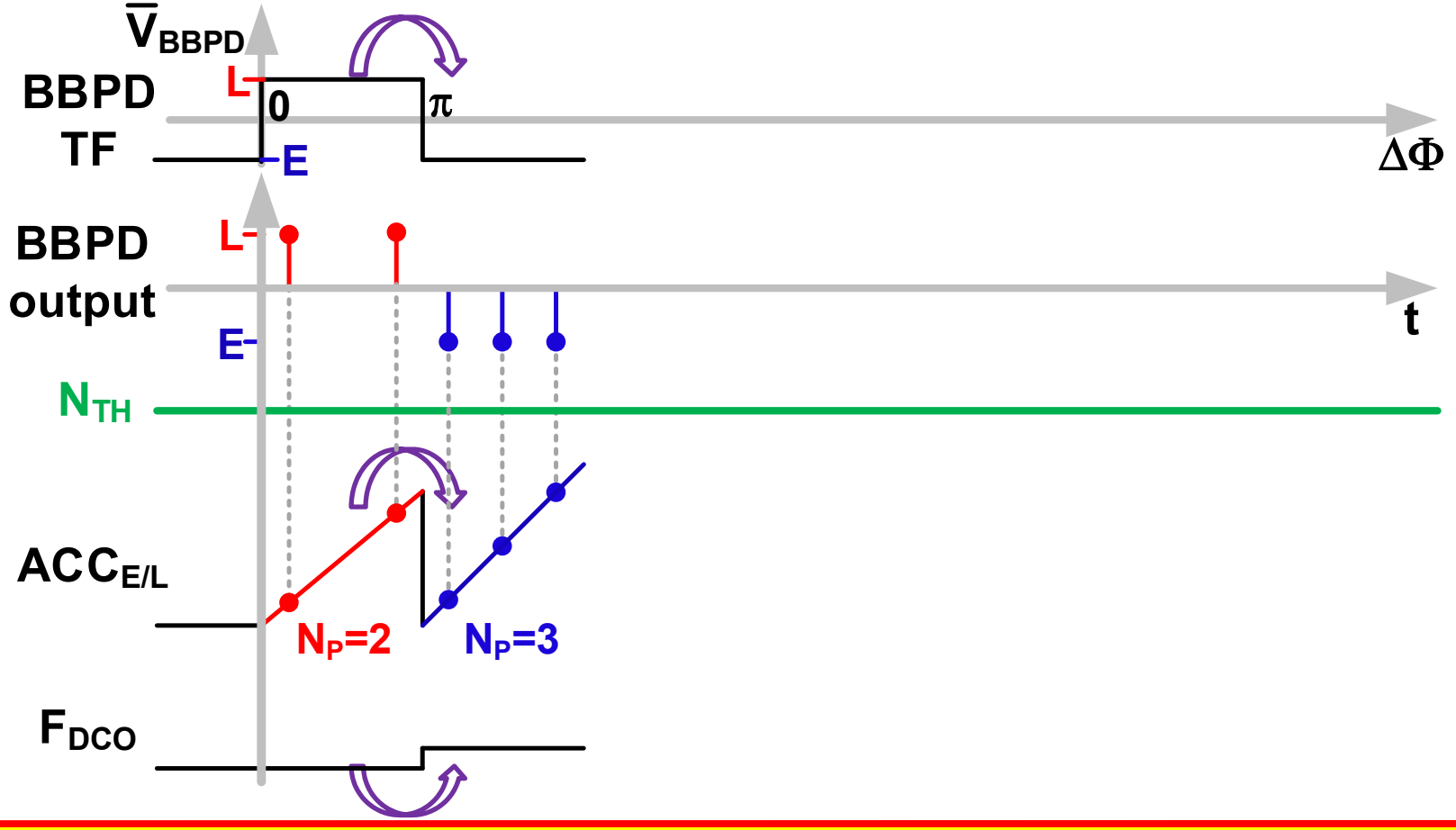
$\Delta F \propto 1/N_P \rightarrow$ Can be used for frequency detection

Proposed BBPD-based FLL



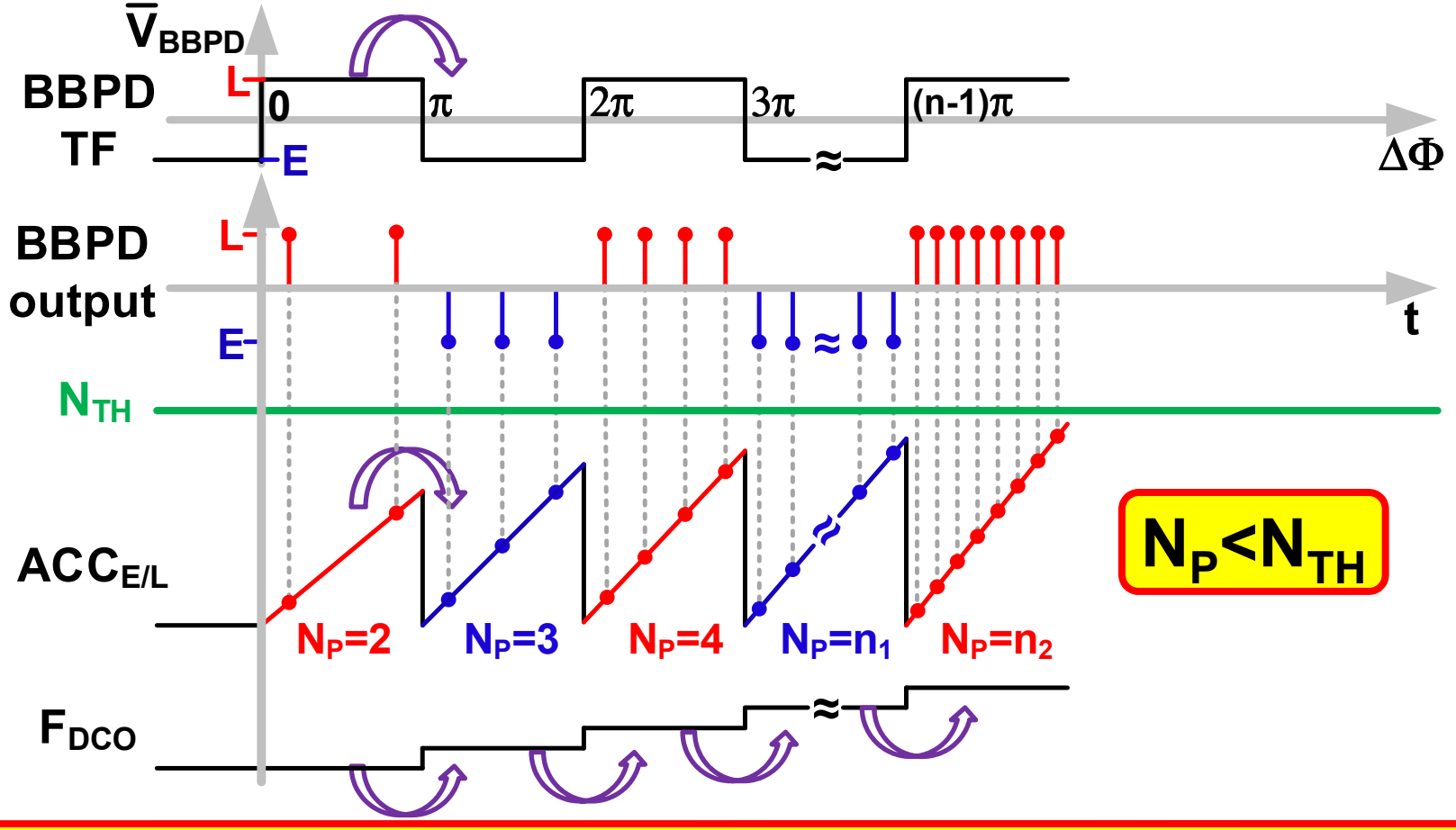
- ✓ No explicit frequency detector
- ✓ Immune to input transition density ρ
- ✓ Unlimited frequency acquisition range

Frequency Acquisition Process



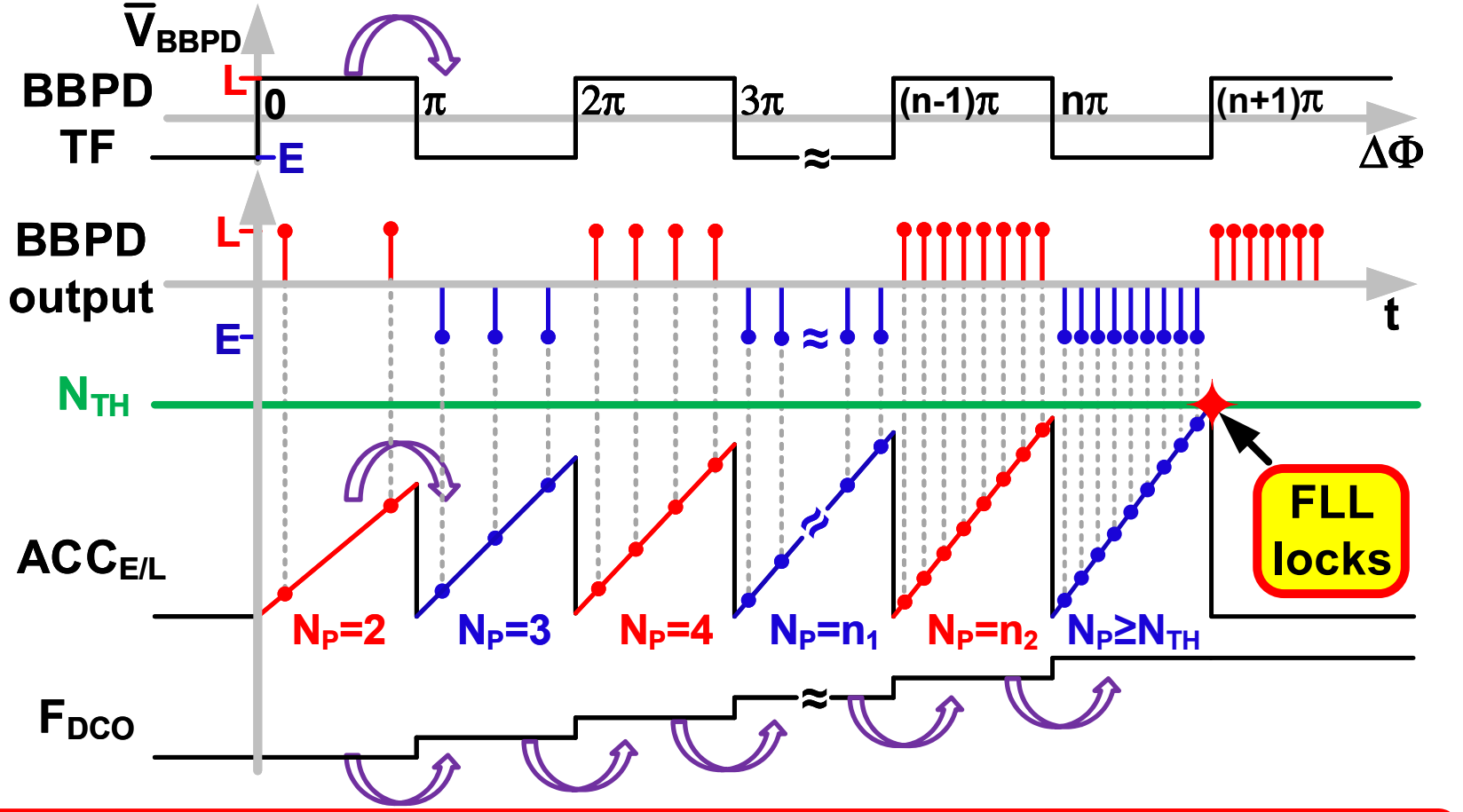
DCO starts from its lowest frequency

Frequency Acquisition Process



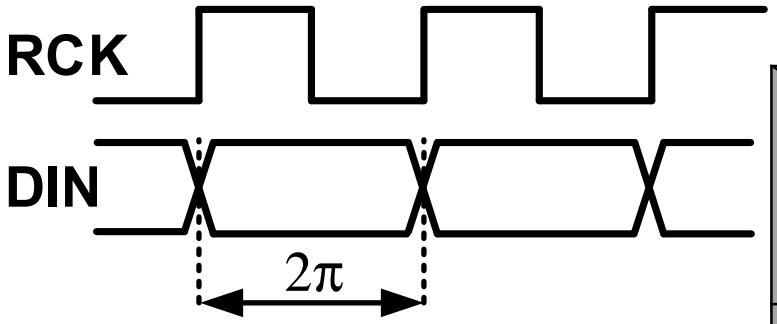
Increment F_{DCO} at each E→L and L→E transition

Frequency Acquisition Process



Lock is achieved when $N_P \geq N_{TH}$

Transition Density Dependence



$$N_P = \rho \frac{F_{DIN}}{\Delta F} \frac{\pi}{2\pi}$$

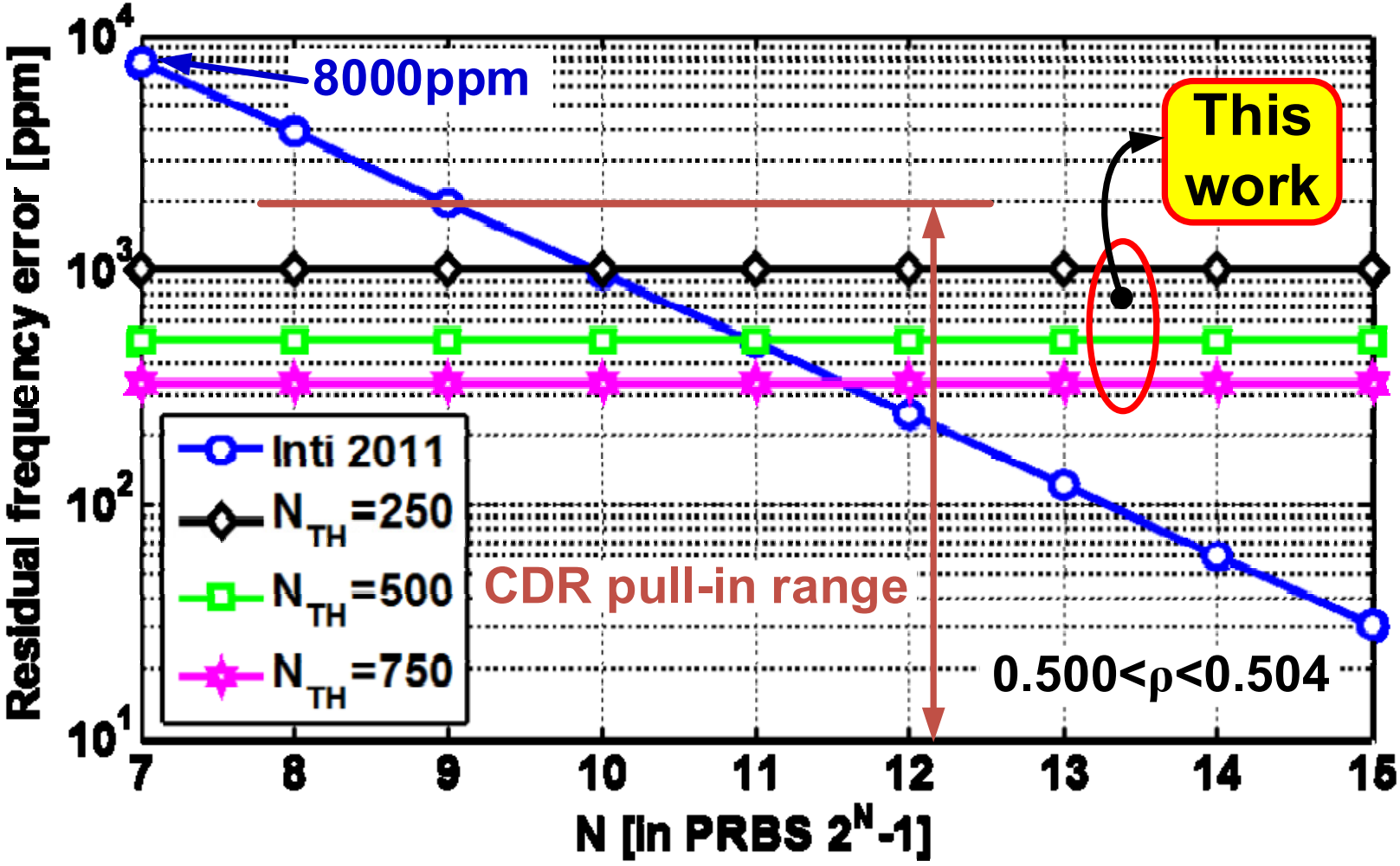
$$\Rightarrow \frac{\Delta F}{F_{DIN}} = \frac{\rho}{N_P} \frac{\pi}{2\pi} = \frac{\rho}{2N_P}$$

$\Delta F/F_{DIN}$ [ppm] \ ρ	0.1	0.5	1.0
N_{TH}=250	200	1000	2000
N_{TH}=500	100	500	1000
N_{TH}=750	66	330	660

$N_{TH}=N_P=500$, $\Delta F \leq 1000$ppm when $0 \leq \rho \leq 1$

Residual Freq. Error Comparison

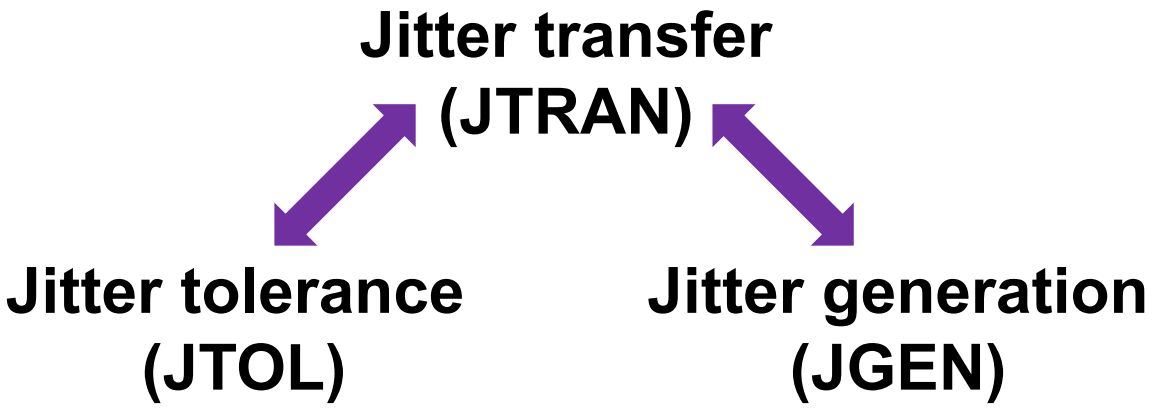
- Proposed scheme is immune to transition density ρ



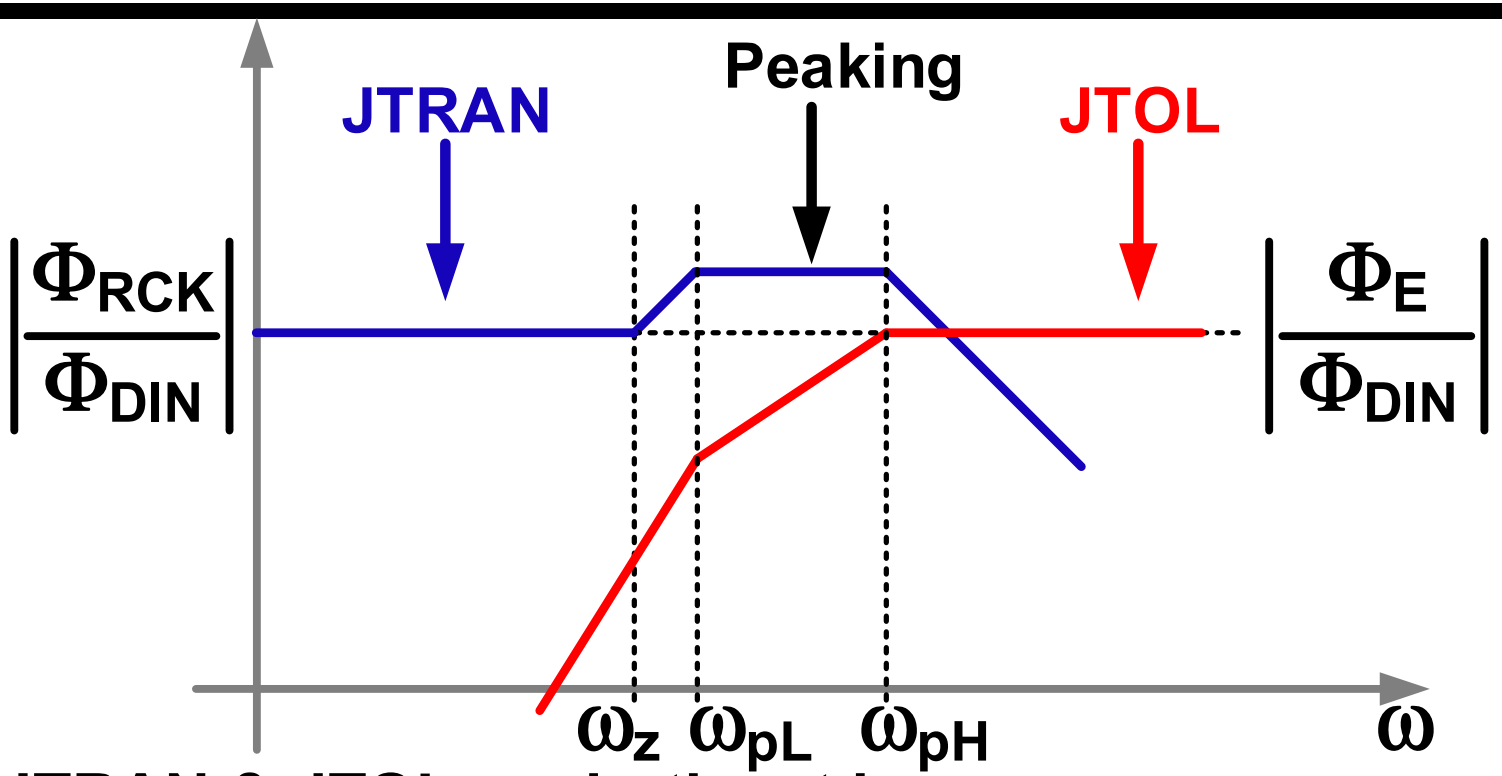
CDR Design Challenges

- Automatic frequency acquisition

- **JTRAN/JTOL/JGEN tradeoffs**

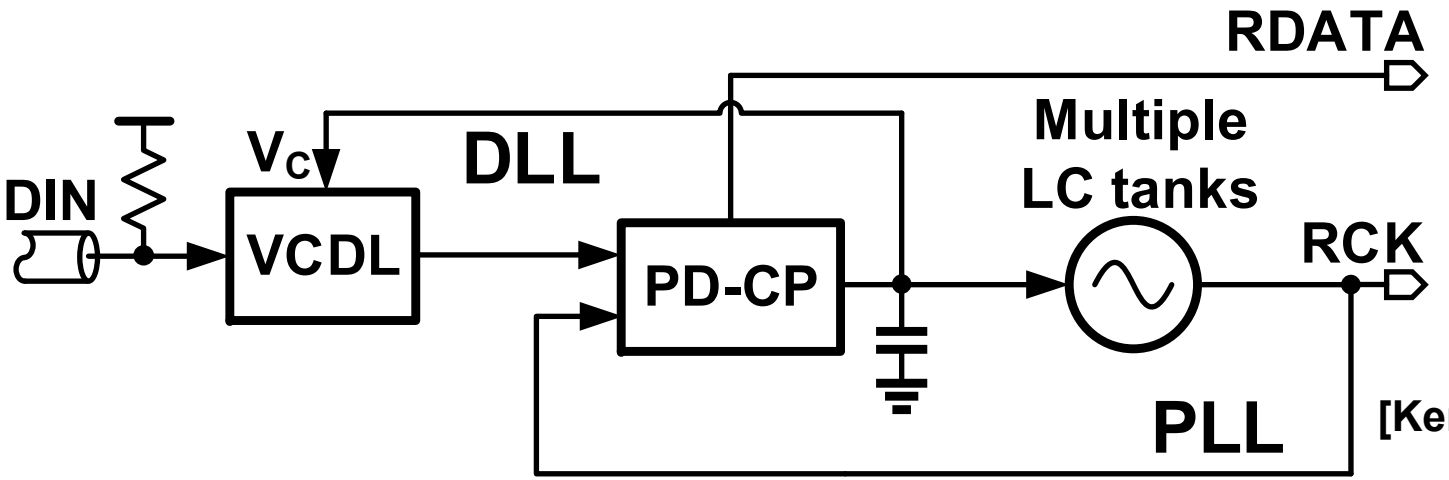


Classical 2nd Order CDR Tradeoffs



- JTRAN & JTOL are both set by ω_{pH}
  - Impossible to achieve low JTRAN with high JTOL
- JTRAN & JGEN conflict
  - Input jitter filtering and VCO noise suppression tradeoff

D/PLL Architecture



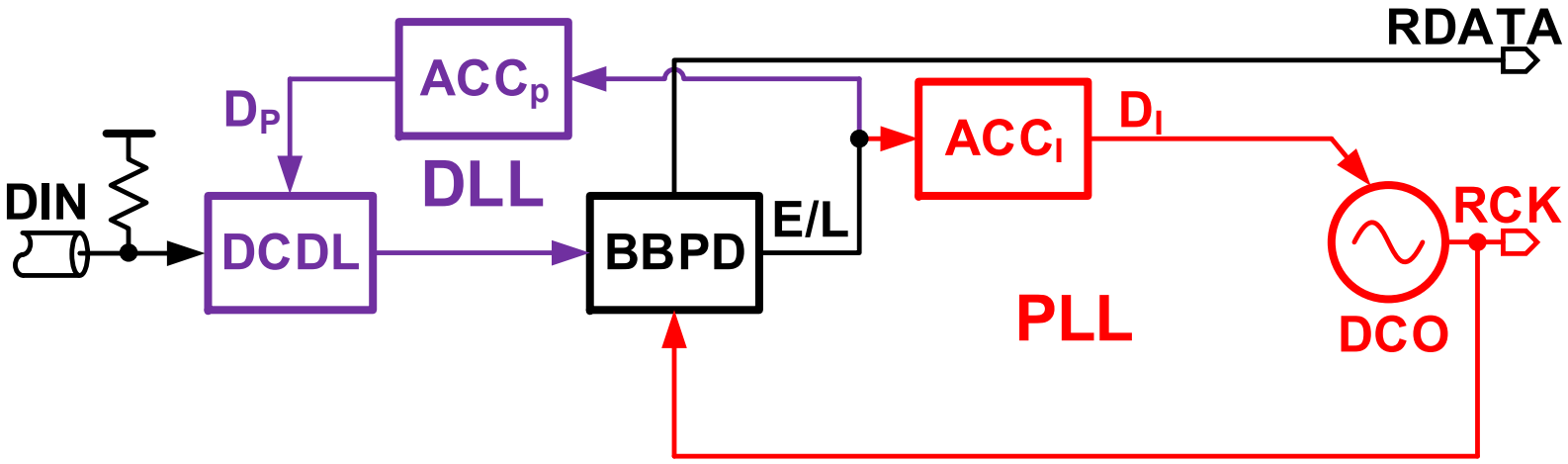
[Kenney, *ISSCC06*]

[Dalton, *ISSCC05*]

[Lee & Bulzacchelli, *ISSCC92*]

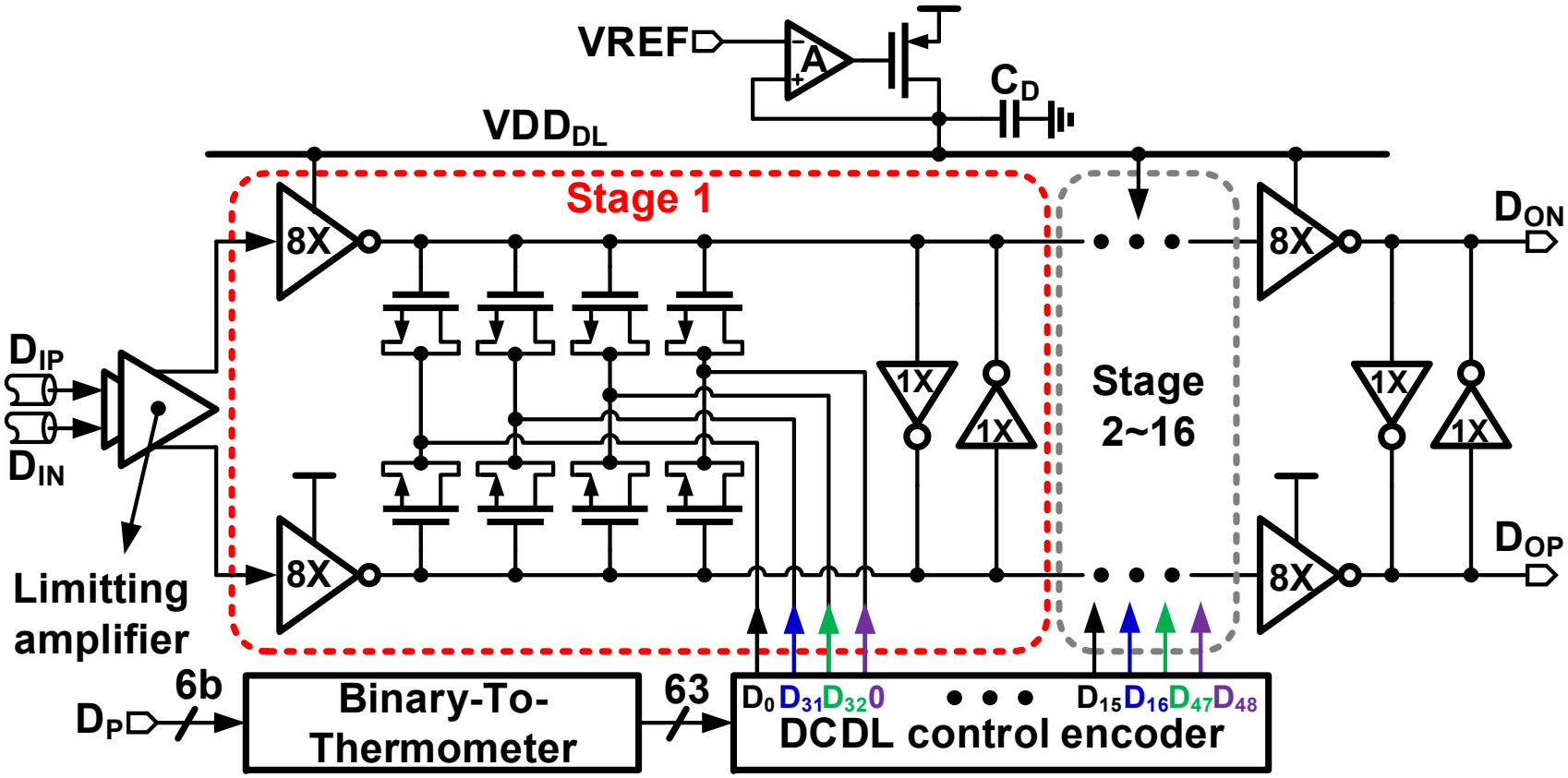
- ✓ **Decouple JTRAN/JTOL**
  - **No jitter peaking**
- × **Power and area overhead**
  - **Multiple LC tanks and CML buffers for VCDL**
- × **Big off-chip loop filter capacitors**

Proposed Digital D/PLL Architecture



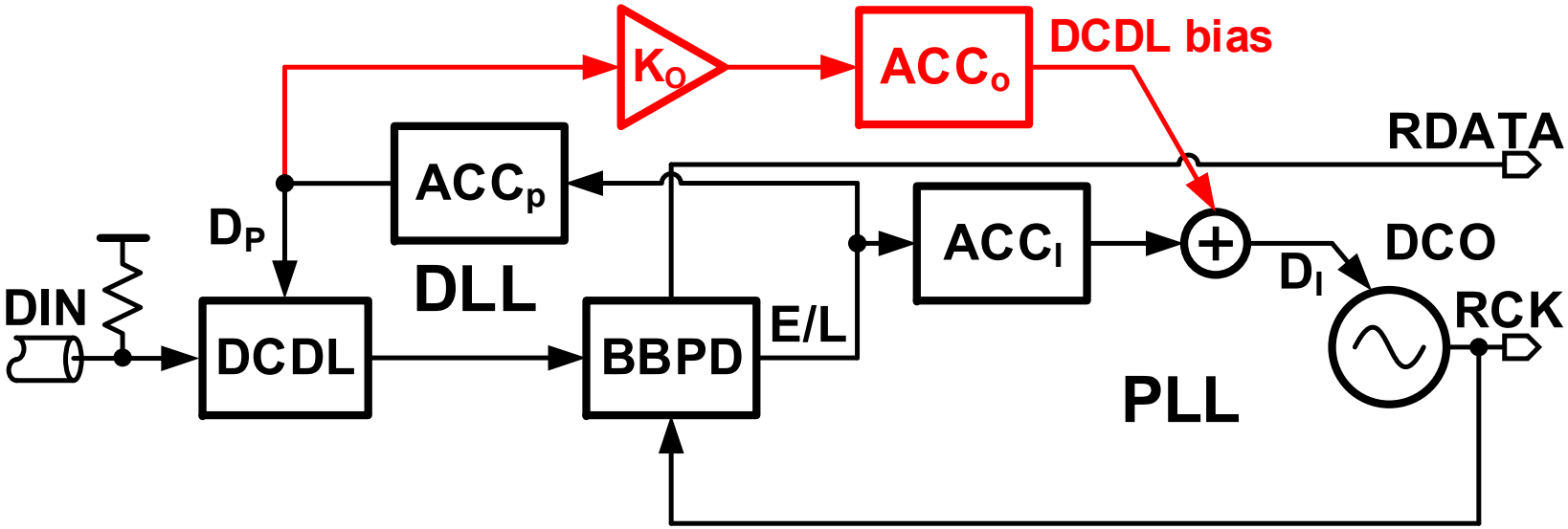
- ✓ **Decoupled JTRAN and JTOL, no jitter peaking**
  - **JTRAN=K_{DCO}/K_{DCDL} (doesn't depend on BBPD gain)**
- ✓ **Wide-range ring oscillator based DCO**
- ✓ **DCDL using CMOS buffers for low power**

Digitally Controlled Delay Line



- 16 stages: about 200ps total delay

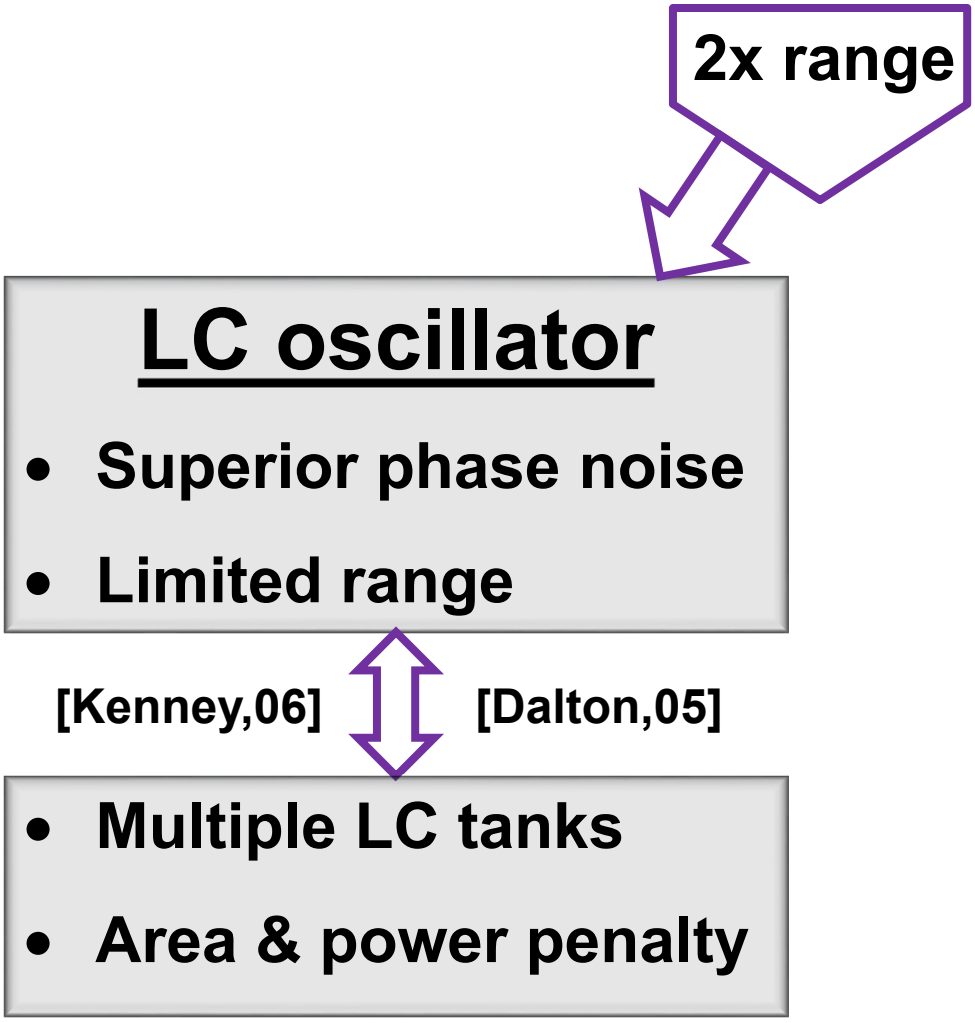
DCDL Bias for JTOL Maximization



- DCDL is biased at mid-delay point in steady state

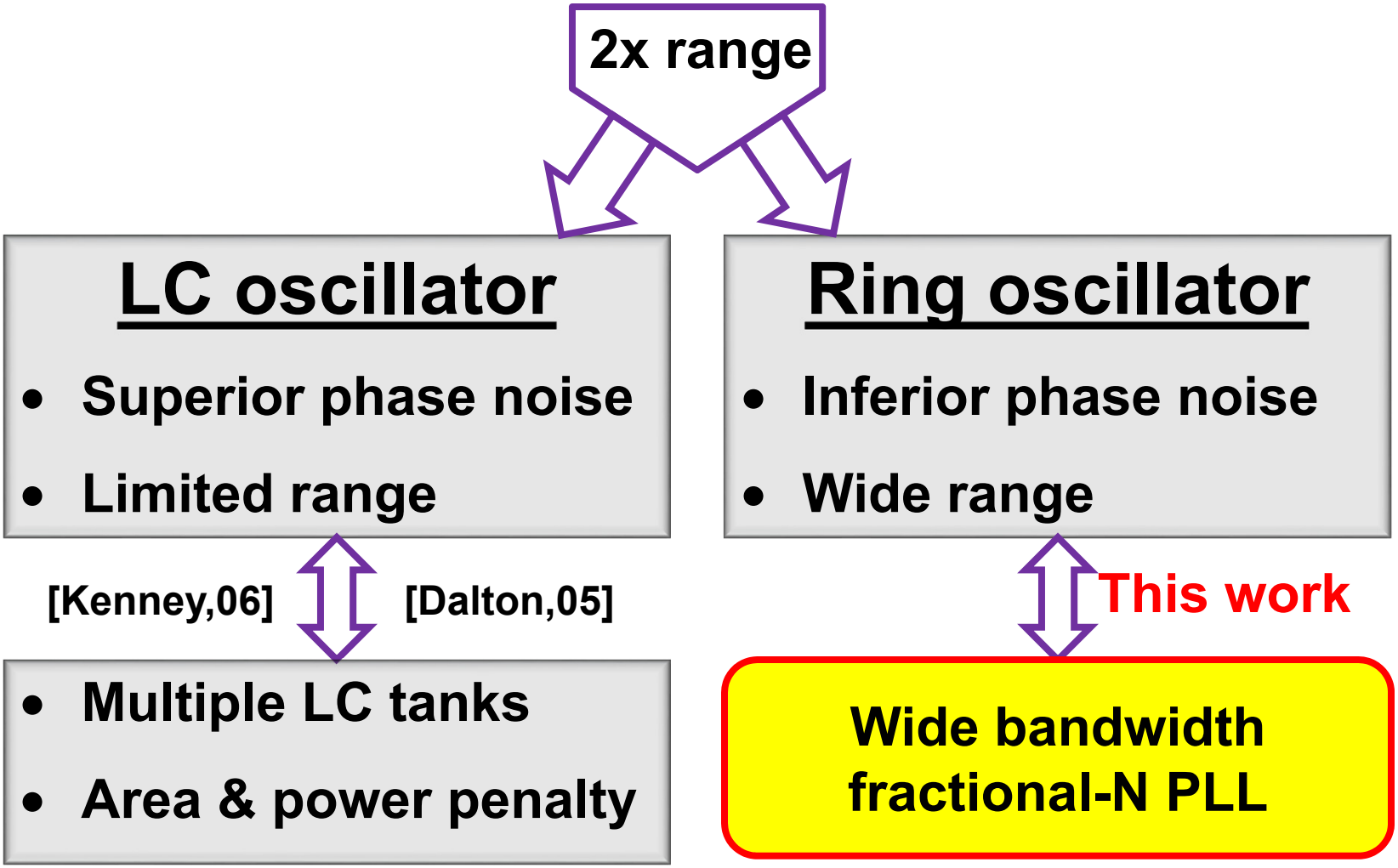
Wide-Range DCO Solution (LC)

- 2x range is required for continuous-rate operation

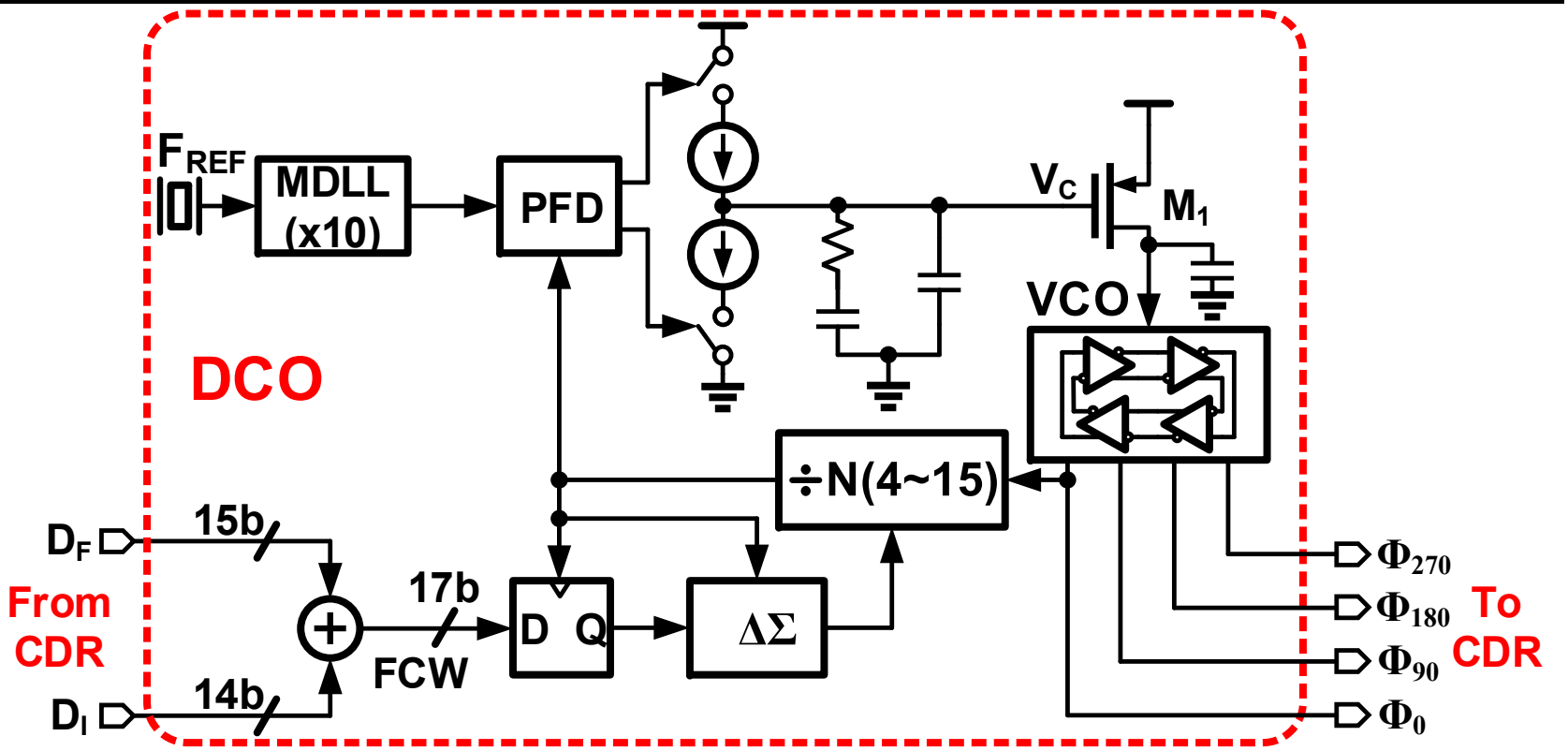


Wide-Range DCO Solution (Ring)

- 2x range is required for continuous-rate operation

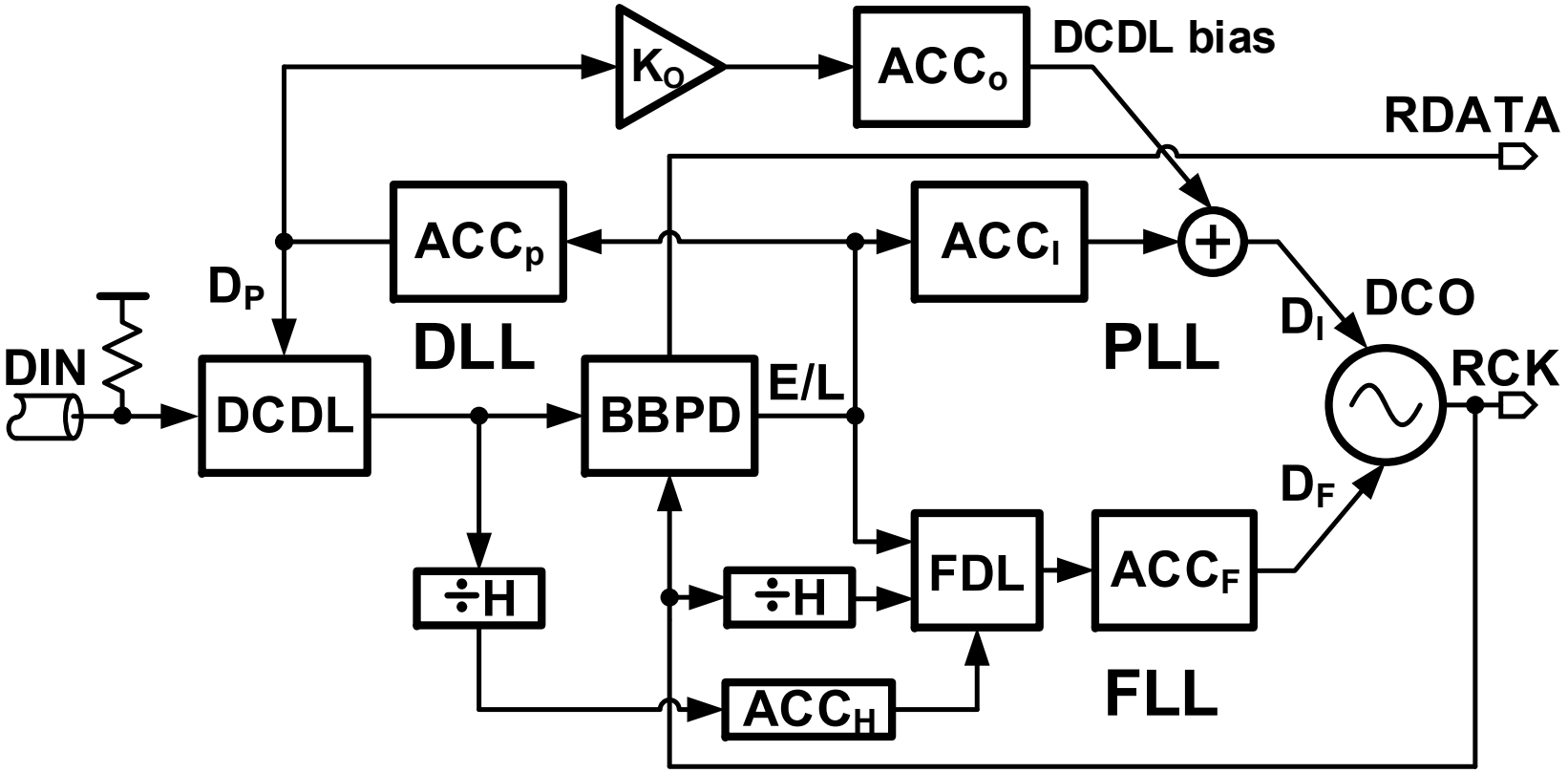


DCO Architecture



- Wide bandwidth PLL to suppress ring VCO noise
- F_{REF} is not related to frequency acquisition

Complete CDR Architecture

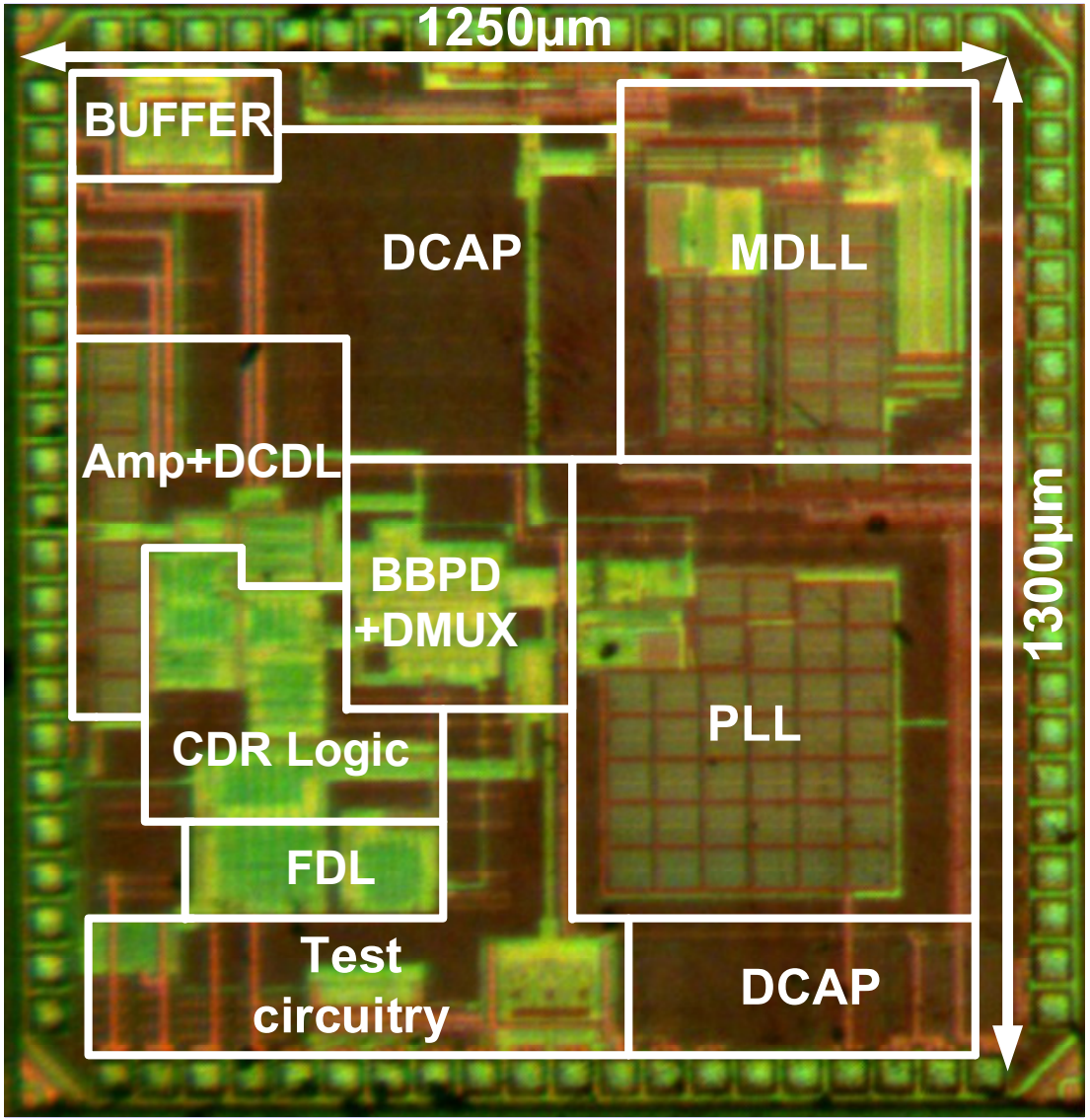


- BBPD-based FLL with immunity to transition density
- Digital D/PLL architecture with fraction-N PLL as DCO

Outline

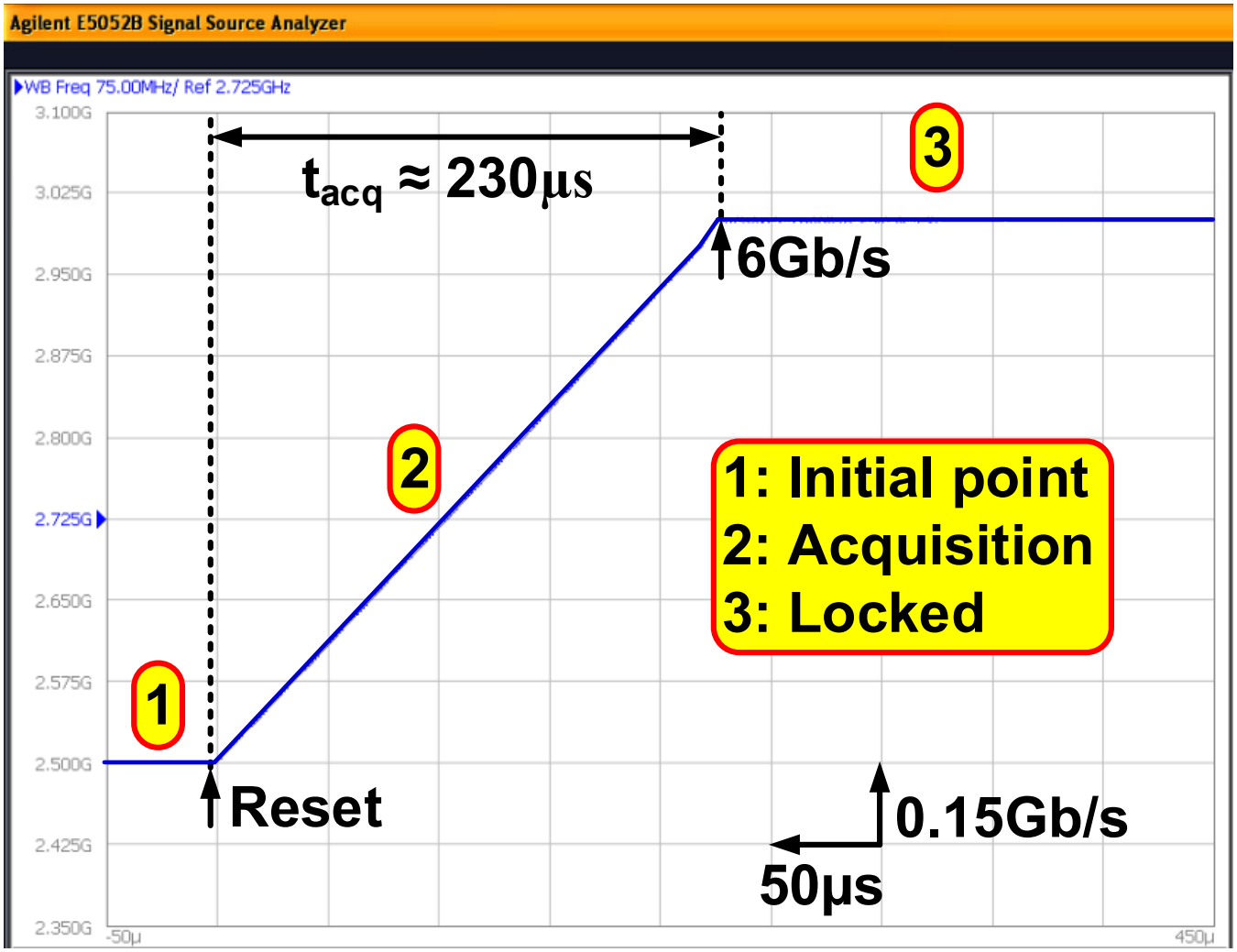
- Introduction
- Automatic Frequency Acquisition
- CDR Architecture
- **Measurement Results**
- Summary

Die Micrograph

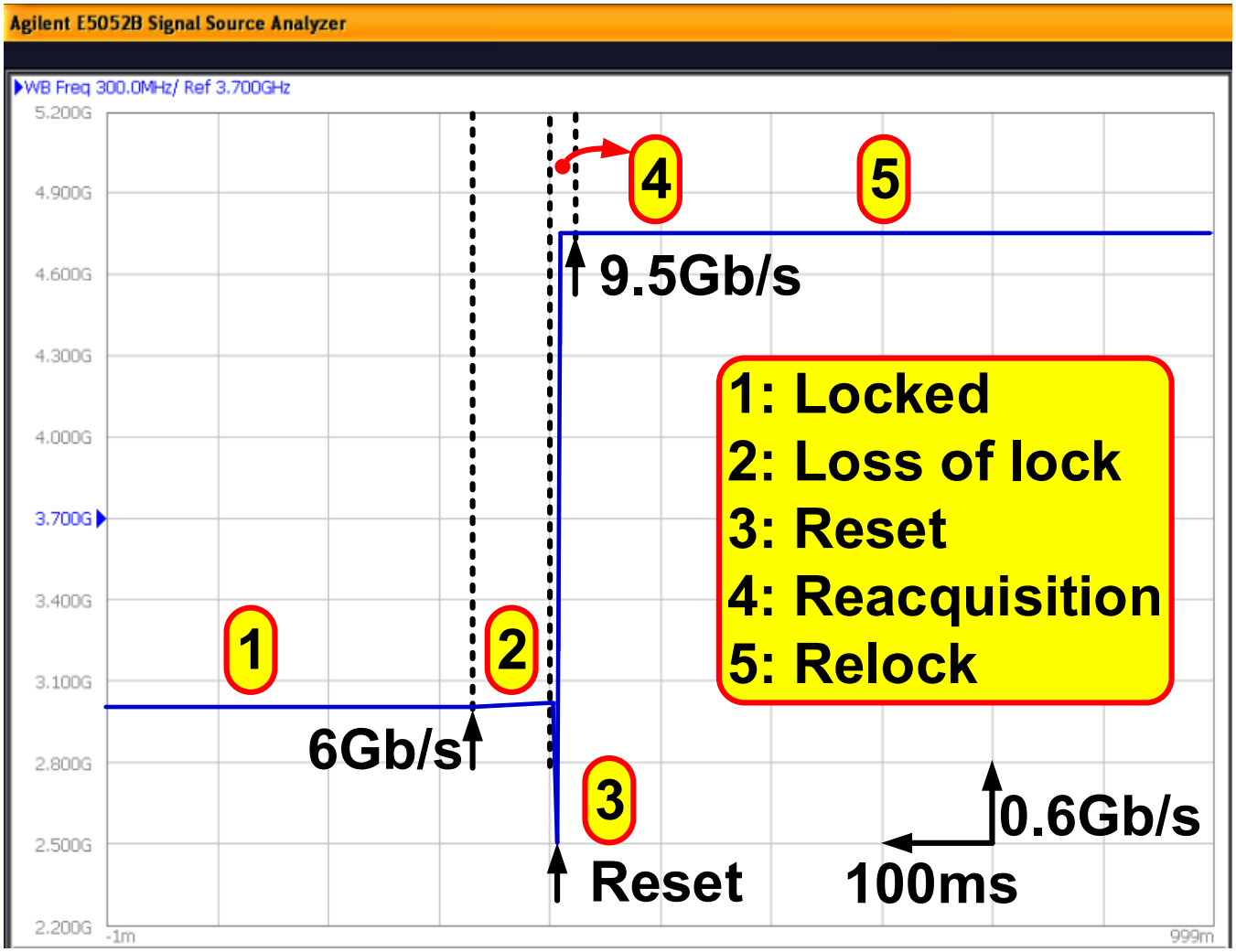


- 65nm CMOS
- Area: 1.63mm^2
- Power:
  22.5mW@10Gb/s
- Data Rate:
  4Gb/s~10.5Gb/s
- QFN88 package

Frequency Acquisition: 6Gb/s

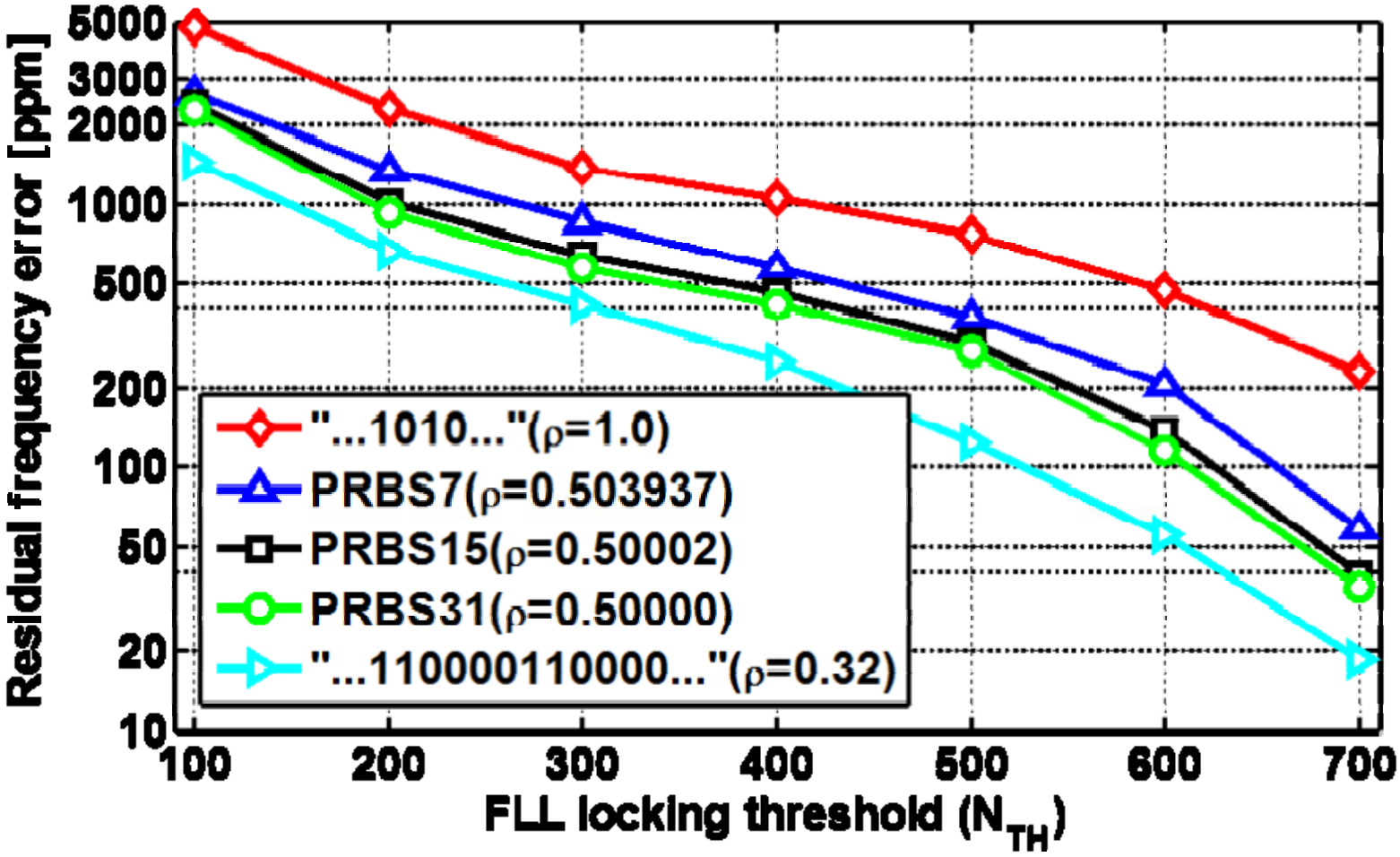


Data Rate Switching: 6Gb/s → 9.5Gb/s



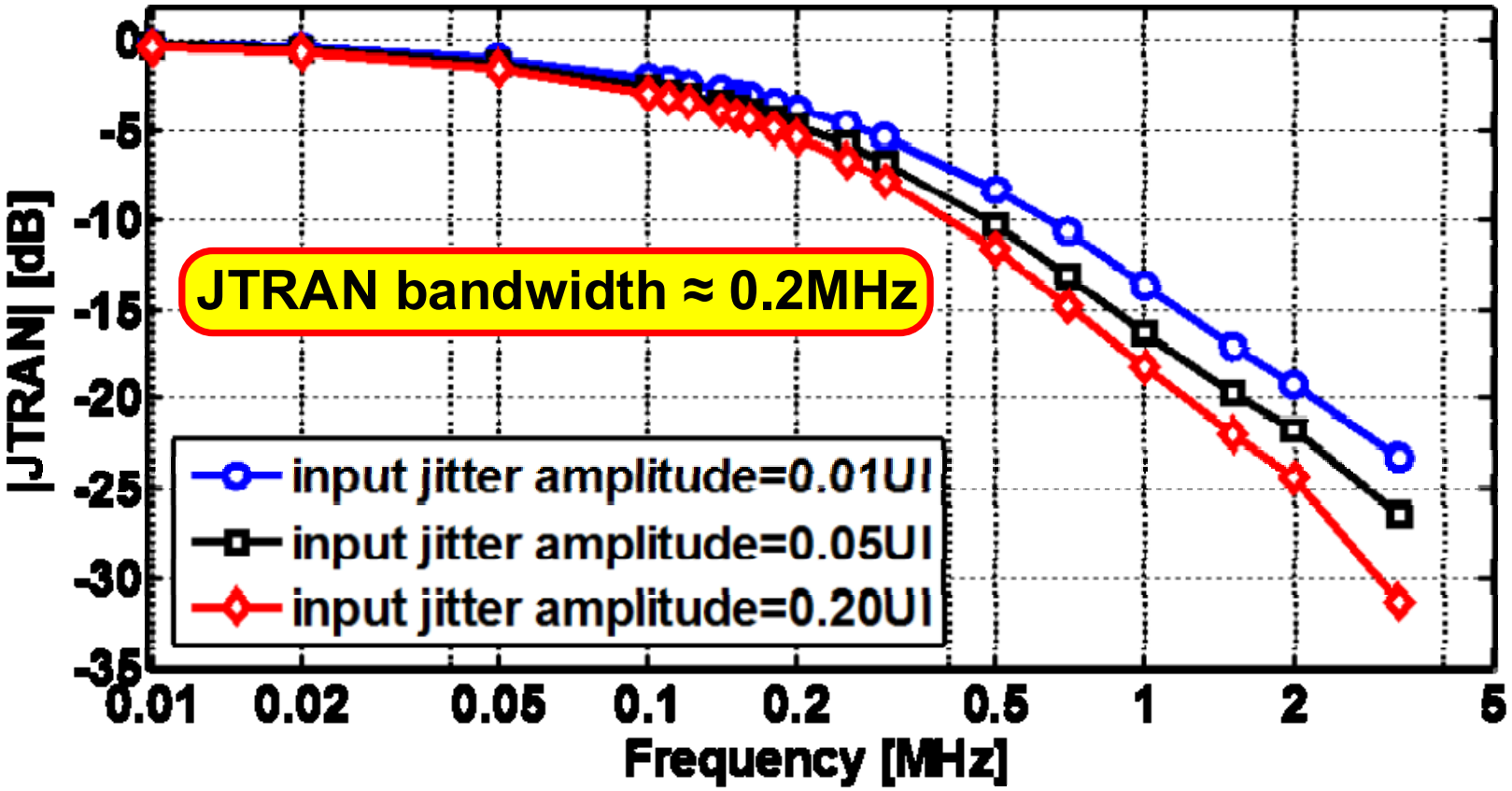
Residual Frequency Error

- N_{TH}>=500, residual frequency error within 1000ppm



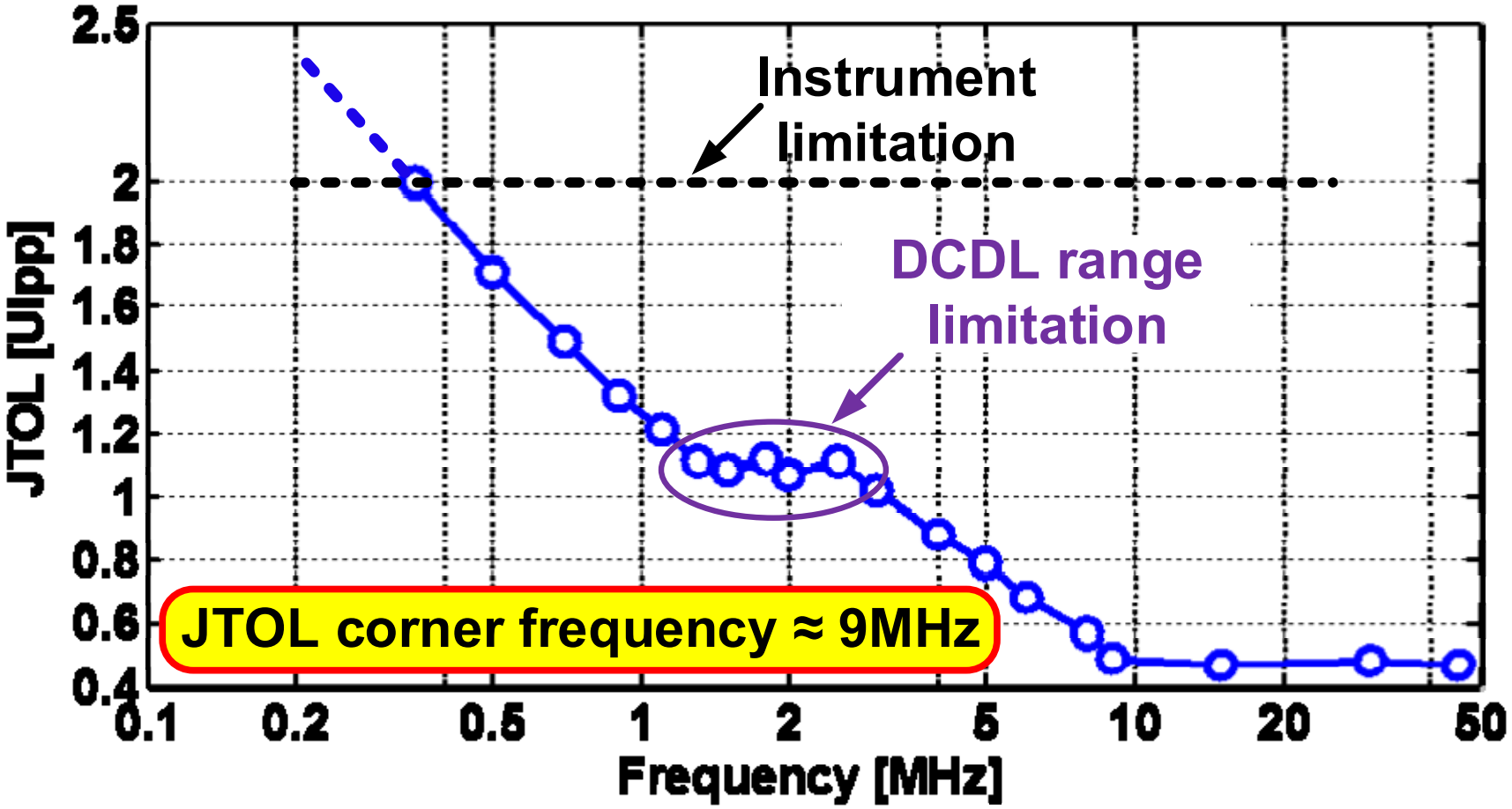
Measured Jitter Transfer (JTRAN)

- JTRAN is independent of input jitter and no peaking

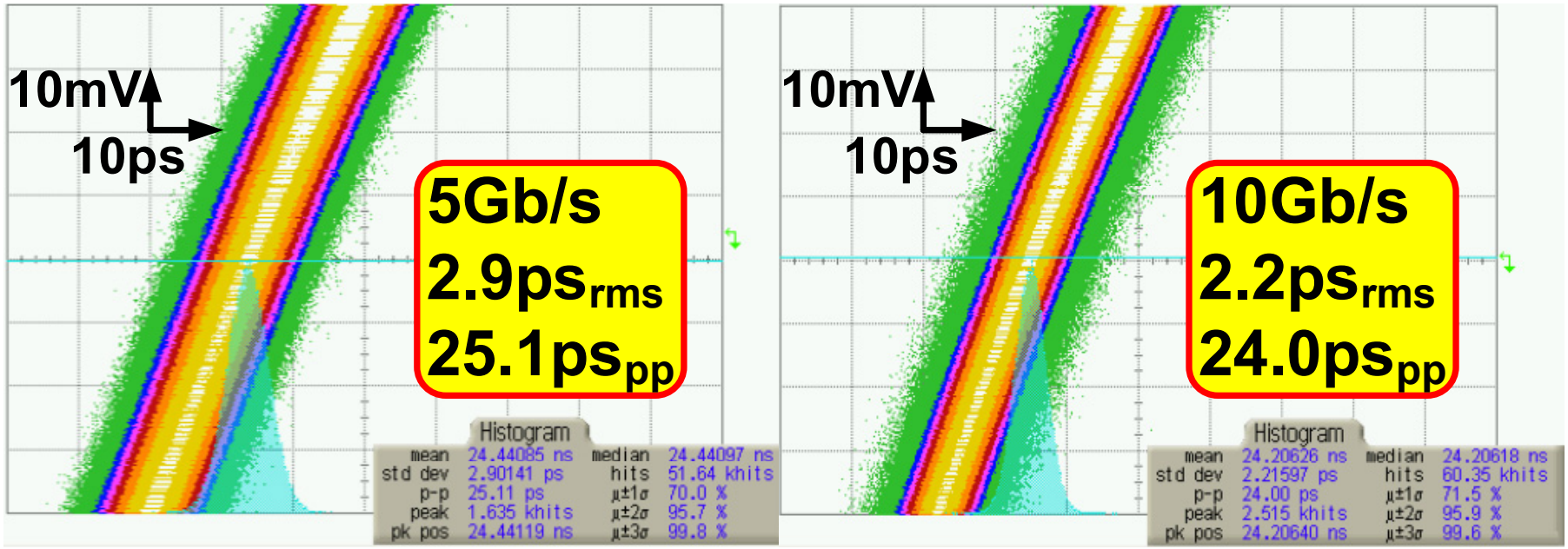


Measured Jitter Tolerance (JTOL)

- DCDL range (about 200ps) limits mid-frequency JTOL

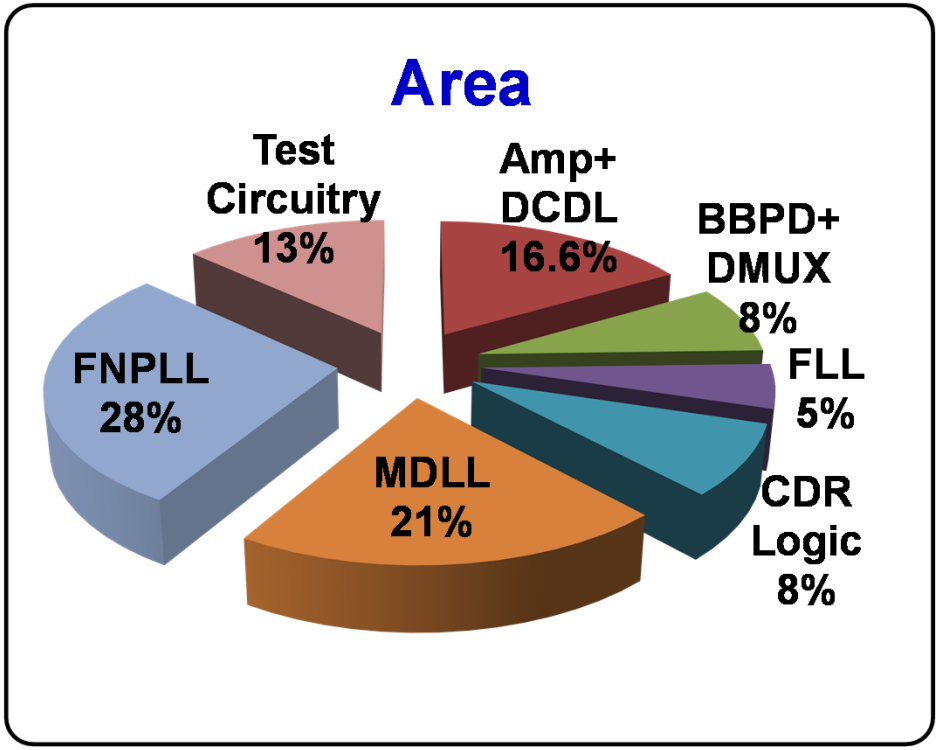


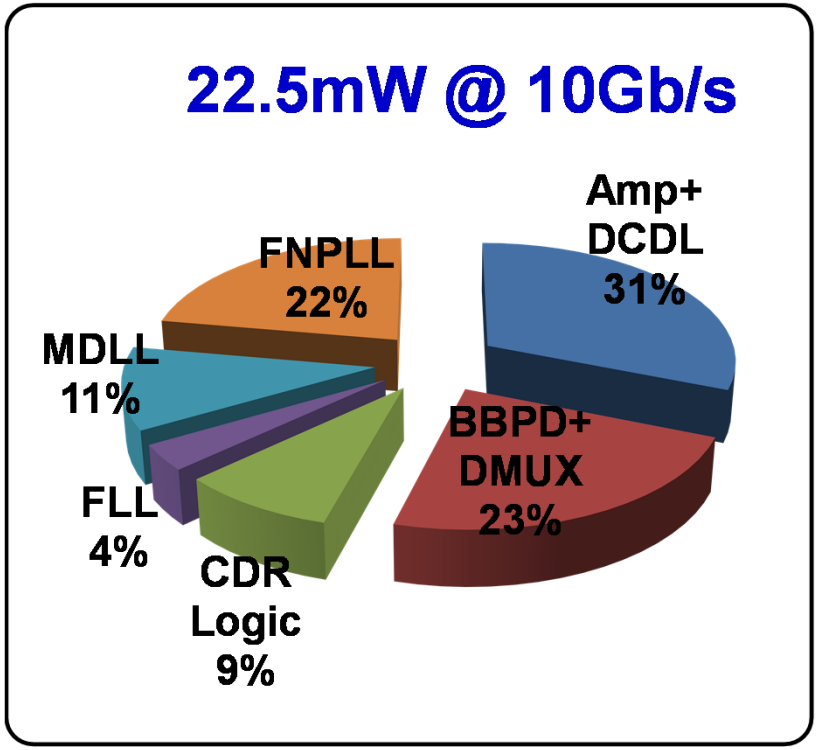
RCK Long-Term Jitter w/ PRBS31 Data



Area & Power Breakdown

- DCO takes about 50% of the area and 30% of the power
  - More efficient than multiple LC tanks





Comparison with State-of-the-art

	ISSCC'05 [2] D. Dalton	ISSCC'06 [3] J. Kenney	ISSCC'11 [1] R. Inti	ISSCC'09 S.-K. Lee	This work
Technology	0.35µm	0.13µm	0.13µm	65nm	65nm
Supply [V]	3.3	3.3/1.8	1.2/0.8	1.2	1.2/1.0
FD type	RFD	Counter	Divider	DLL	BBPD
Architecture	Full-rate	Half-rate	Half-rate	Full-rate	Half-rate
Oscillator	LC	LC	Ring	Ring	Ring
JTRAN[MHz]	0.5	1.2	N/A	N/A	0.2
Jitter [ps_{rms}/ps_{pp}]	0.4/8.0	0.5/4.5	5.4/44.0	9.7/53.3	2.2/24.0
Data rate [Gb/s]	0.0125-2.7	9.95-11.3	0.5-2.5	0.65-8	4-10.5
Power [mW]	775@2.5Gb/s	800@11.4Gb/s	6.1@2.1Gb/s	88.6@8Gb/s	22.5@10Gb/s
FoM [mW/Gb/s]	310.2	70.2	3.05	11.08	2.25
Area [mm^2]	9.0	8.0	0.39	0.11	1.63

Summary

- *Automatic frequency acquisition*
  - *BBPD-based frequency detection*
  - *Immune to transition density ρ*
- *Eliminate JTRAN/JTOL/JGEN tradeoffs*
  - *Removes big off-chip loop filter capacitor*
  - *Decouples JTRAN/JTOL, no jitter peaking*
  - *Fractional-N PLL as wide-range low-noise DCO*

Acknowledgements

- *Intel Labs University Research Office*
- *Kawasaki Microelectronics America, Inc.*
- *National Science Foundation (NSF) under CAREER EECS-0954969*
- *Berkeley Design Automation (BDA) for Analog Fast Spice (AFS) simulator*
- *Twisted Traces Inc. and Seong-Joong Kim provided testing assistance*

An 8.2Gb/s-to-10.3Gb/s Full-Rate Linear Referenceless CDR Without Frequency Detector in 0.18μm CMOS

Sui Huang[1], Jun Cao[2], and Michael M. Green[1]

[1]University of California, Irvine

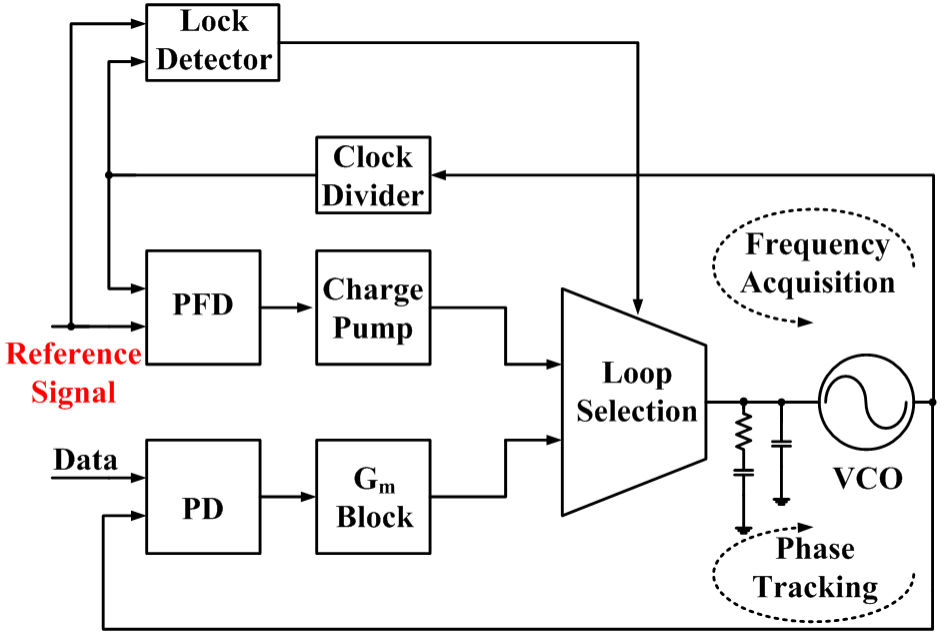
[2]Broadcom Corp., Irvine

Outline

- Introduction
- Analysis of Capture Range of Linear CDRs
- A Full-Rate Linear Referenceless CDR Without Frequency Detector
- Measurement Results and Conclusions

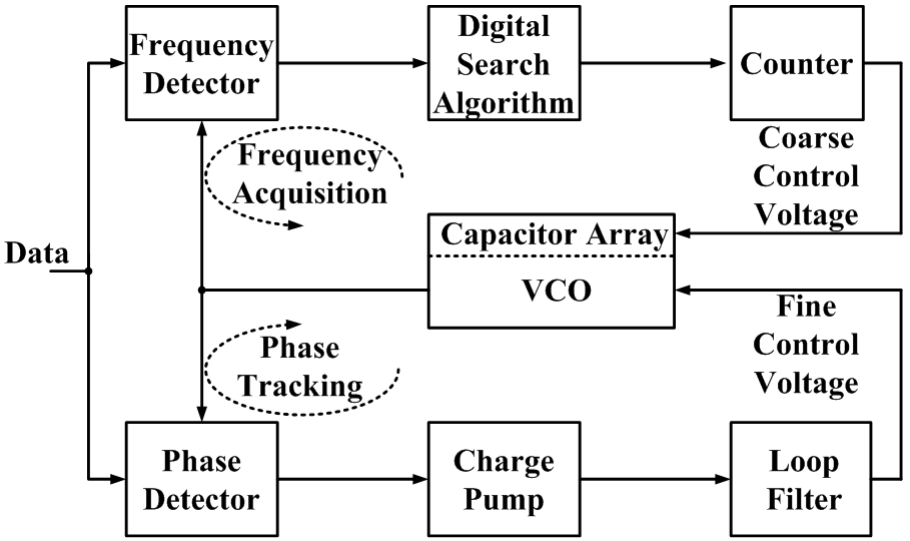
Conventional CDR Architectures

Dual-Loop:



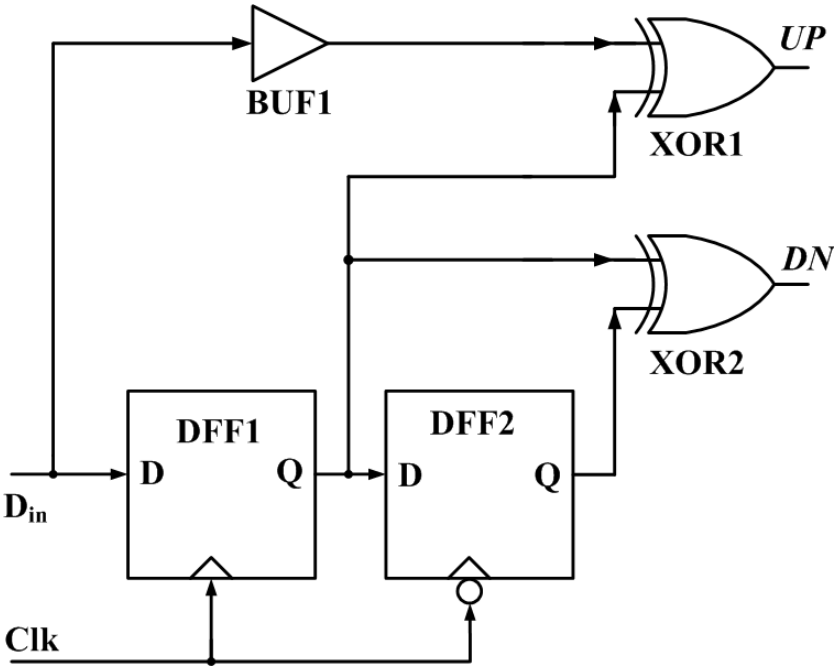
- External reference signal required, which limits applications

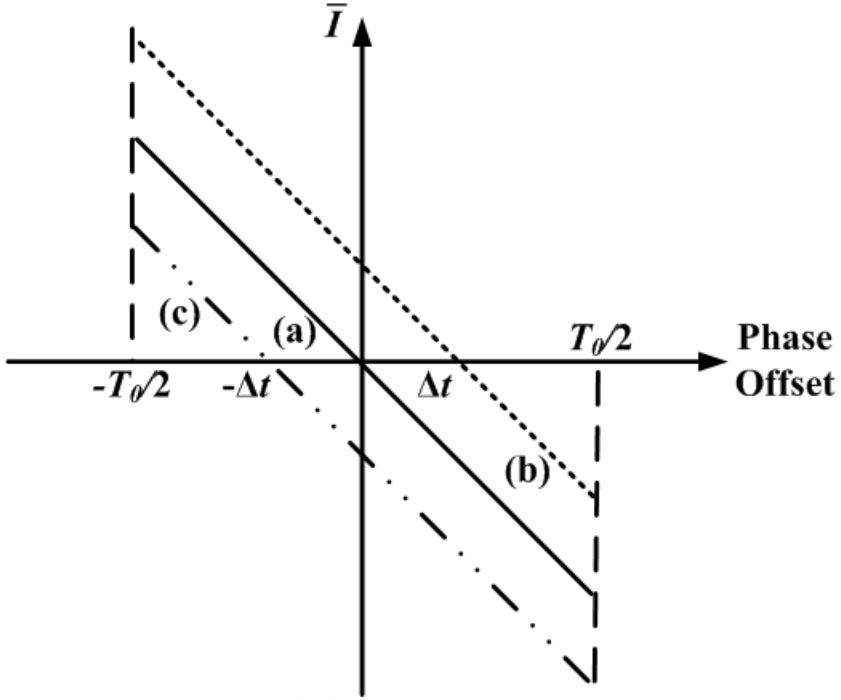
Referenceless:



- Transition between the two loops is not always robust.
- Frequency detector dissipates significant power.

Hogge Phase Detector



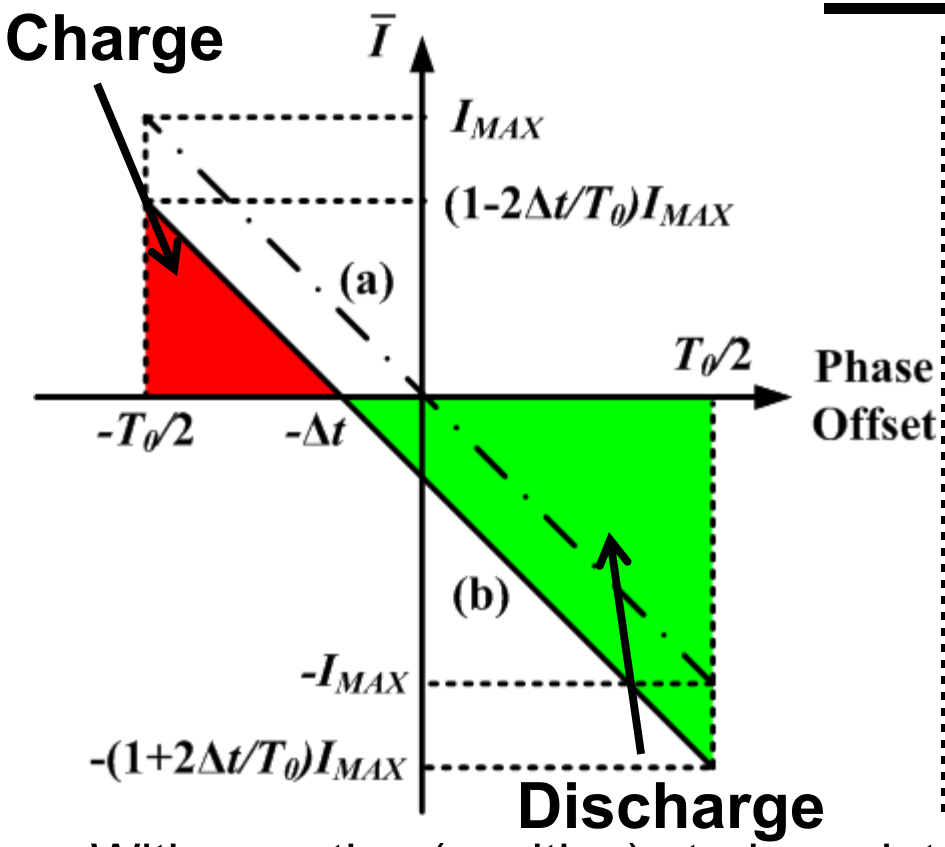


$$\bar{I} = K_{PD}[\Delta\Phi + (t_{DFF1} - t_{BUF1}) + (t_{DFF1} - t_{DFF2})]$$

$\bar{I}$ is the average output current of the phase detector.

- Best jitter performance after locking
- Very sensitive to the delay mismatch among BUF1, DFF1, and DFF2

Capture Range with A Strobe Point



$$\bar{I} \approx \frac{{T_0}^2 |K_{PD}|^2 K_{LF} K_{VCO}}{16\Delta f}\left(1 - \frac{4\Delta t^2}{{T_0}^2}\right) - |K_{PD}|\Delta t$$

where $\Delta f \equiv f_{data} - f_{VCO}$

For $f_{vco} < f_{data}$ ($\Delta f > 0$):

$\bar{I} > 0$ needed for locking

$$\Rightarrow 0 < \Delta f < \frac{T_0 |K_{PD}| K_{LF} K_{VCO}}{8}\left[\frac{T_0/2}{\Delta t} - \frac{\Delta t}{T_0/2}\right]$$

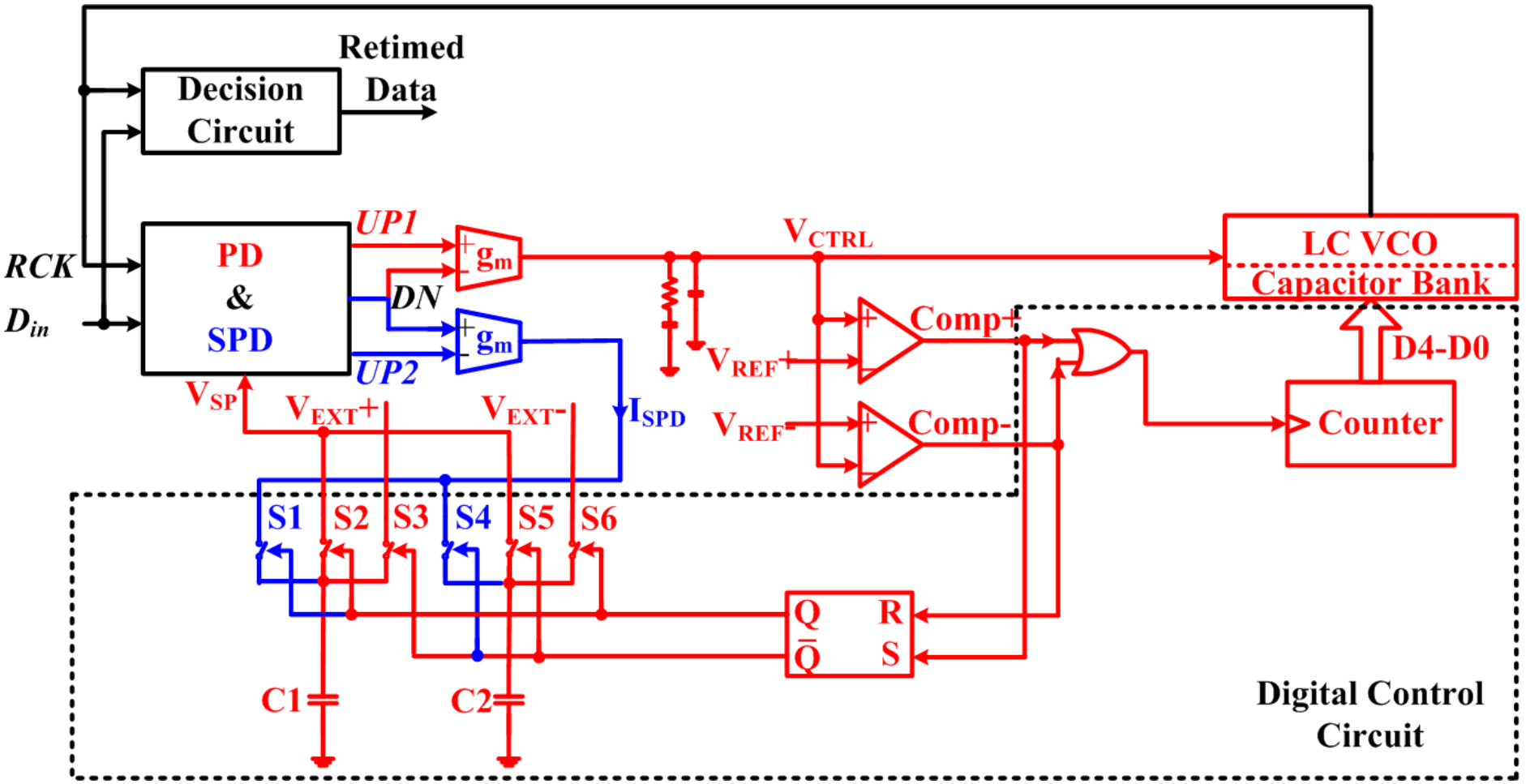
For $f_{vco} > f_{data}$ ($\Delta f < 0$) :

$\bar{I} < 0$ needed for locking

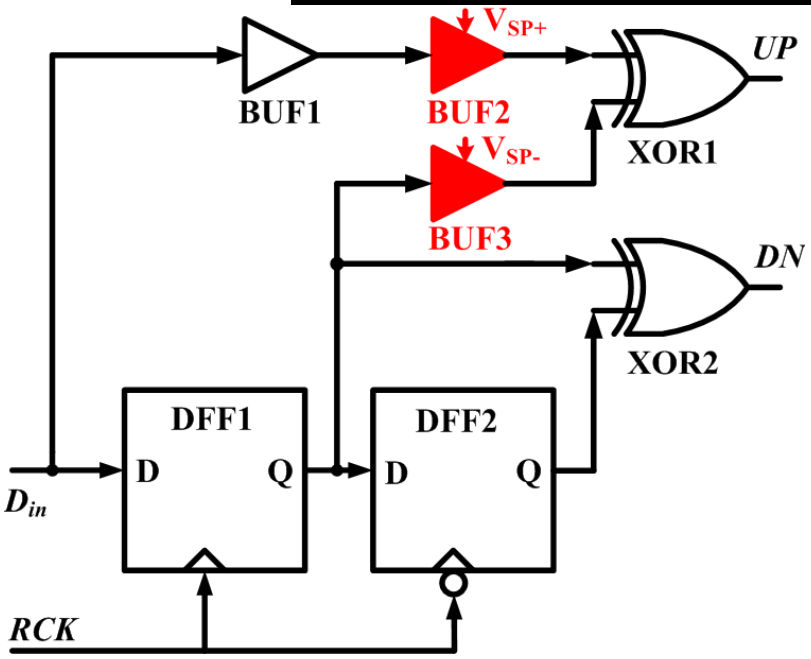
$$\Rightarrow \Delta f < 0 < \frac{T_0 |K_{PD}| K_{LF} K_{VCO}}{8}\left[\frac{T_0/2}{\Delta t} - \frac{\Delta t}{T_0/2}\right]$$

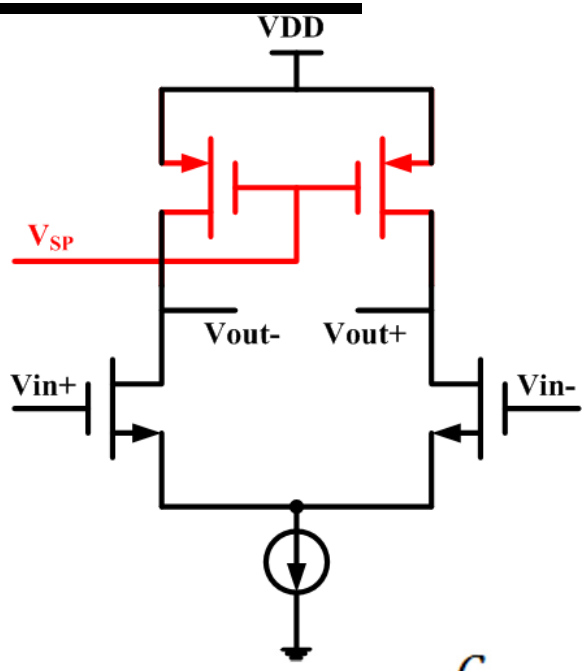
- With negative (positive) strobe point and $\Delta f < 0$ ($\Delta f > 0$) the *single-sided capture range* is very large.
- By switching the strobe point polarity appropriately, locking can be guaranteed.

Referenceless CDR Architecture



Linear Phase Detector With Adjustable Strobe Point





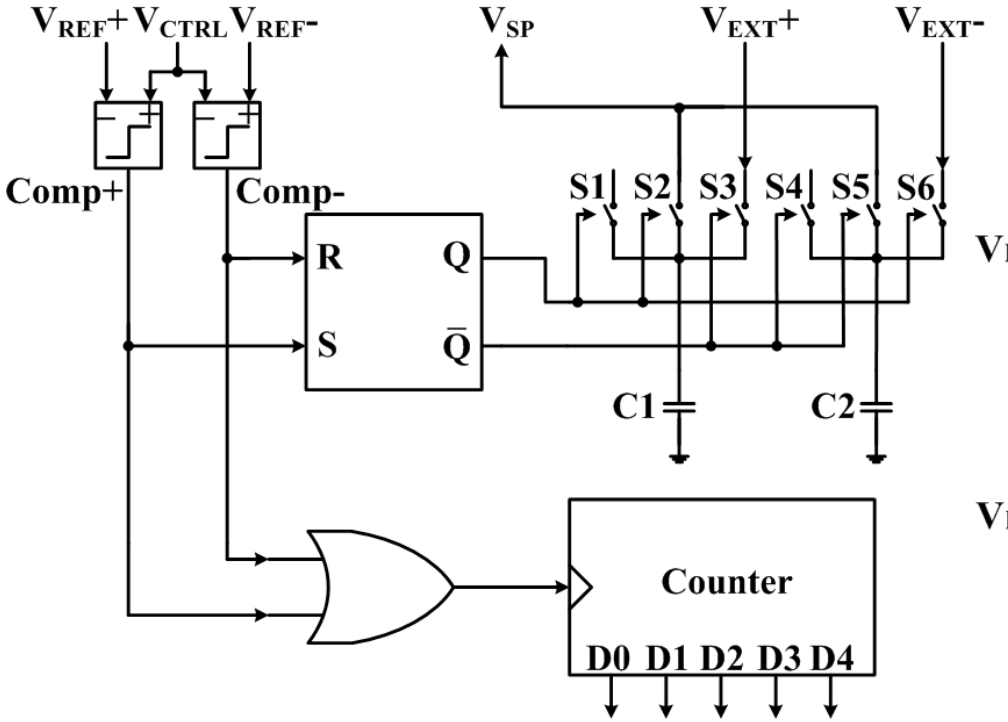
$$\bar{I} = K_{PD}[\Delta\Phi + (t_{DFF1} - t_{BUF1}) + (t_{DFF1} - t_{DFF2}) + (t_{BUF3} - t_{BUF2})]$$

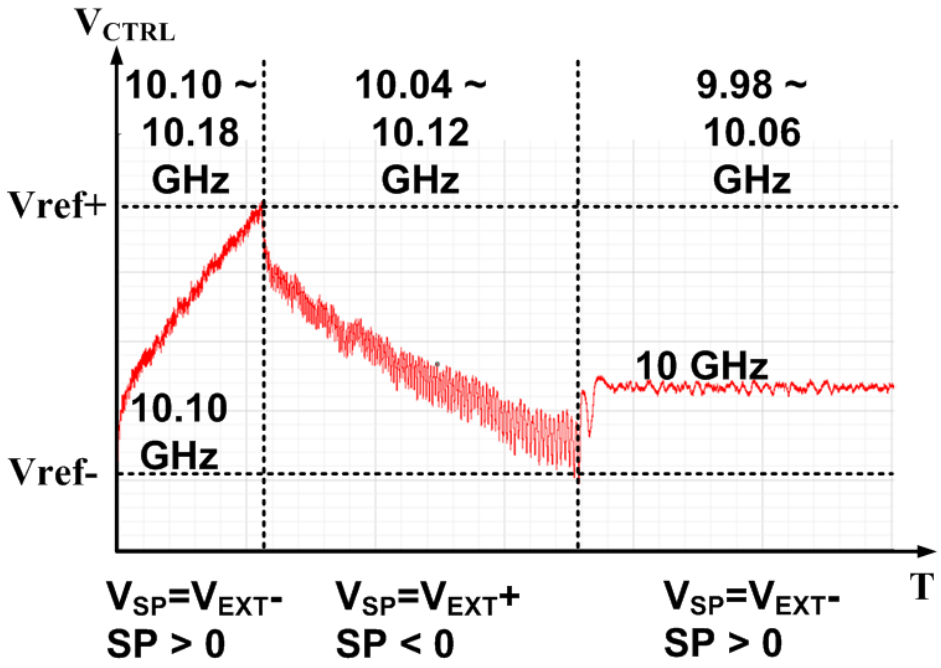
$$t_{delay} = ln2 \cdot \frac{C}{\mu_p C_{ox} \frac{W}{L} (VDD - V_{SP} - |V_{TH}|)}$$

$V_{SP} = V_{SP+} - V_{SP-} > 0$ ⇒ Negative strobe point and larger capture range if f_{VCO} > input bit rate

$V_{SP} = V_{SP+} - V_{SP-} < 0$ ⇒ Positive strobe point and larger capture range if f_{VCO} < input bit rate

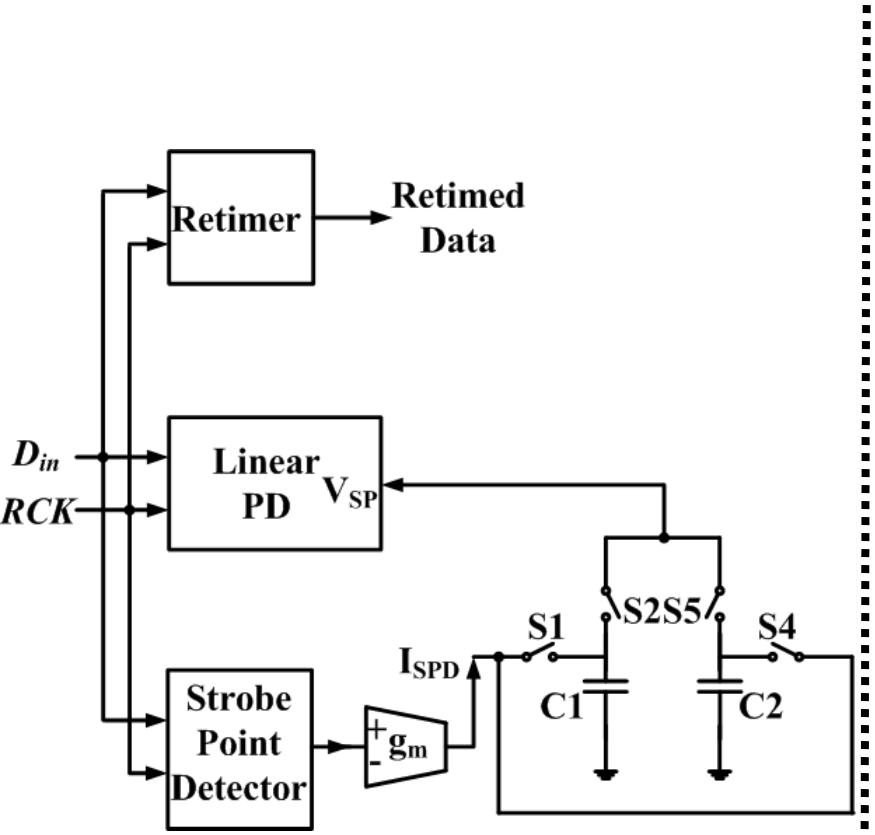
Frequency Acquisition Mode (FAM)

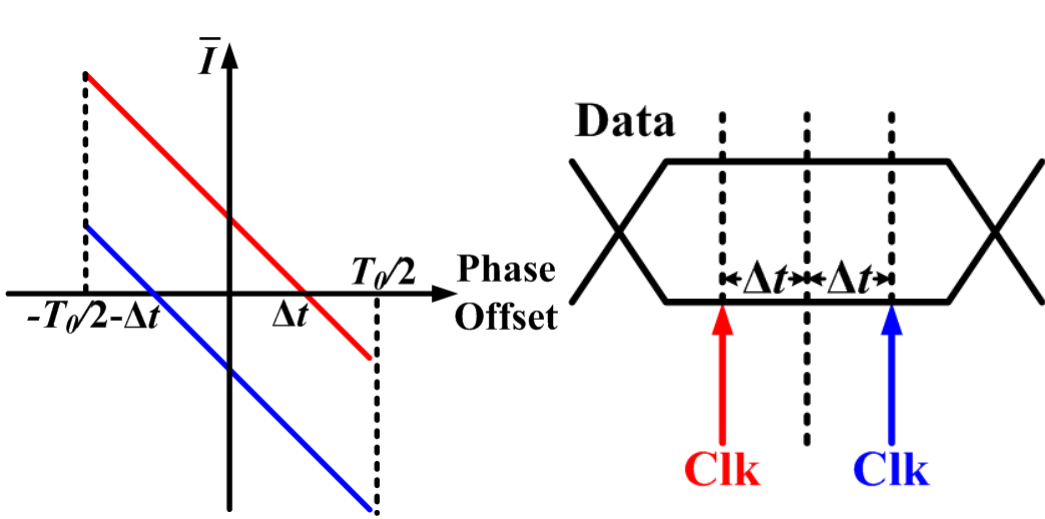


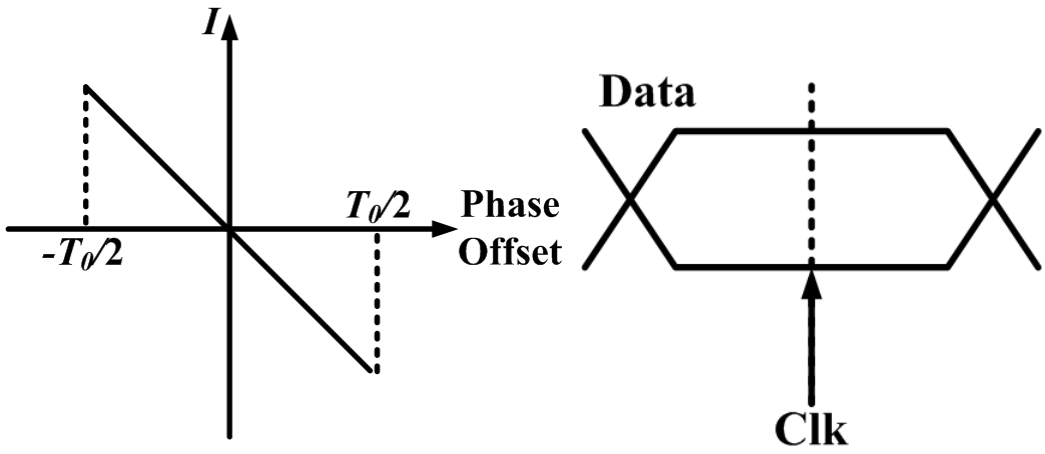


- The strobe point switches its polarity when the VCO shifts from one band to the other.
- The VCO scans through the bands until the CDR is locked at the correct band.

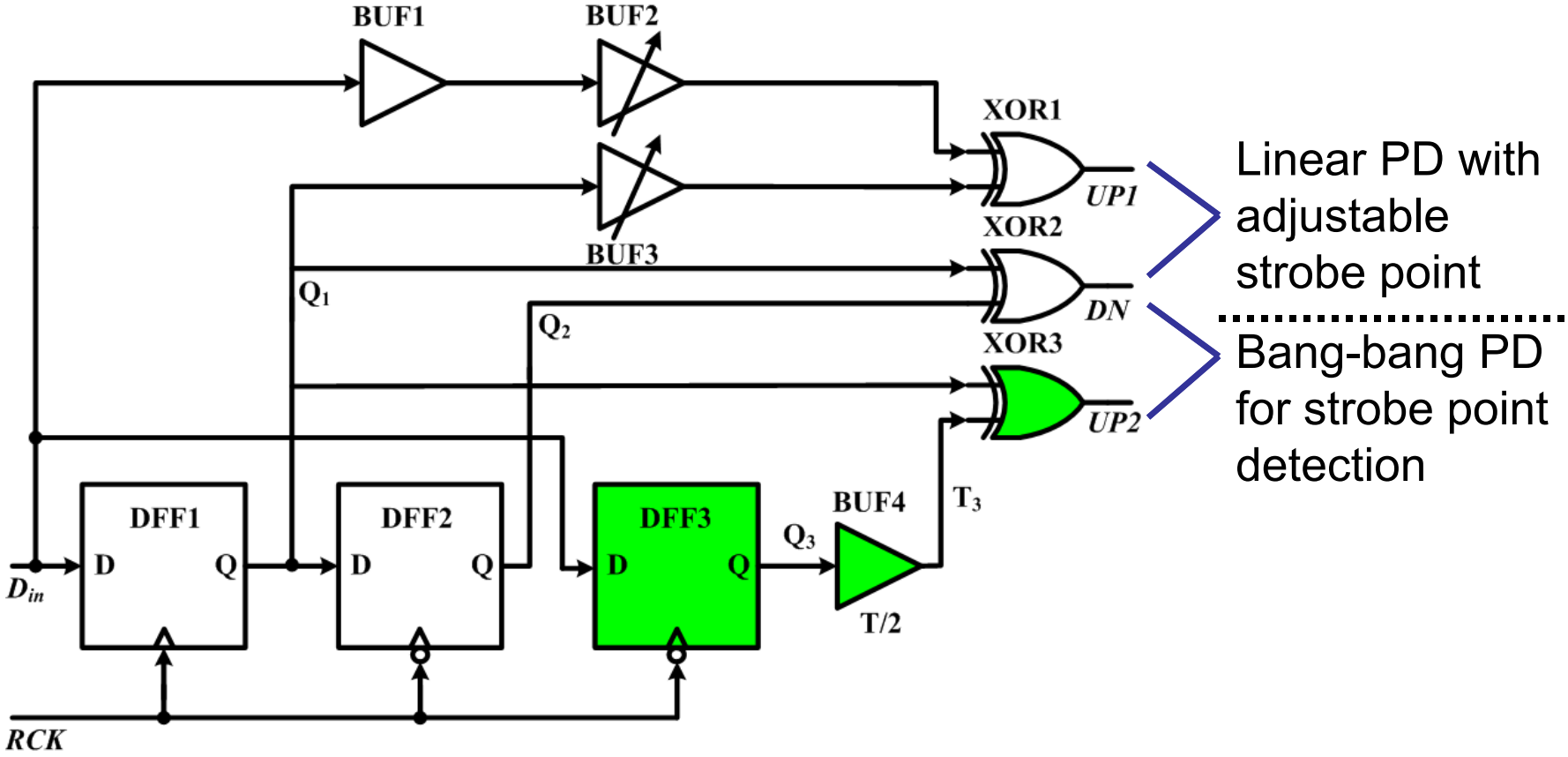
Phase Adjustment Mode (PAM)





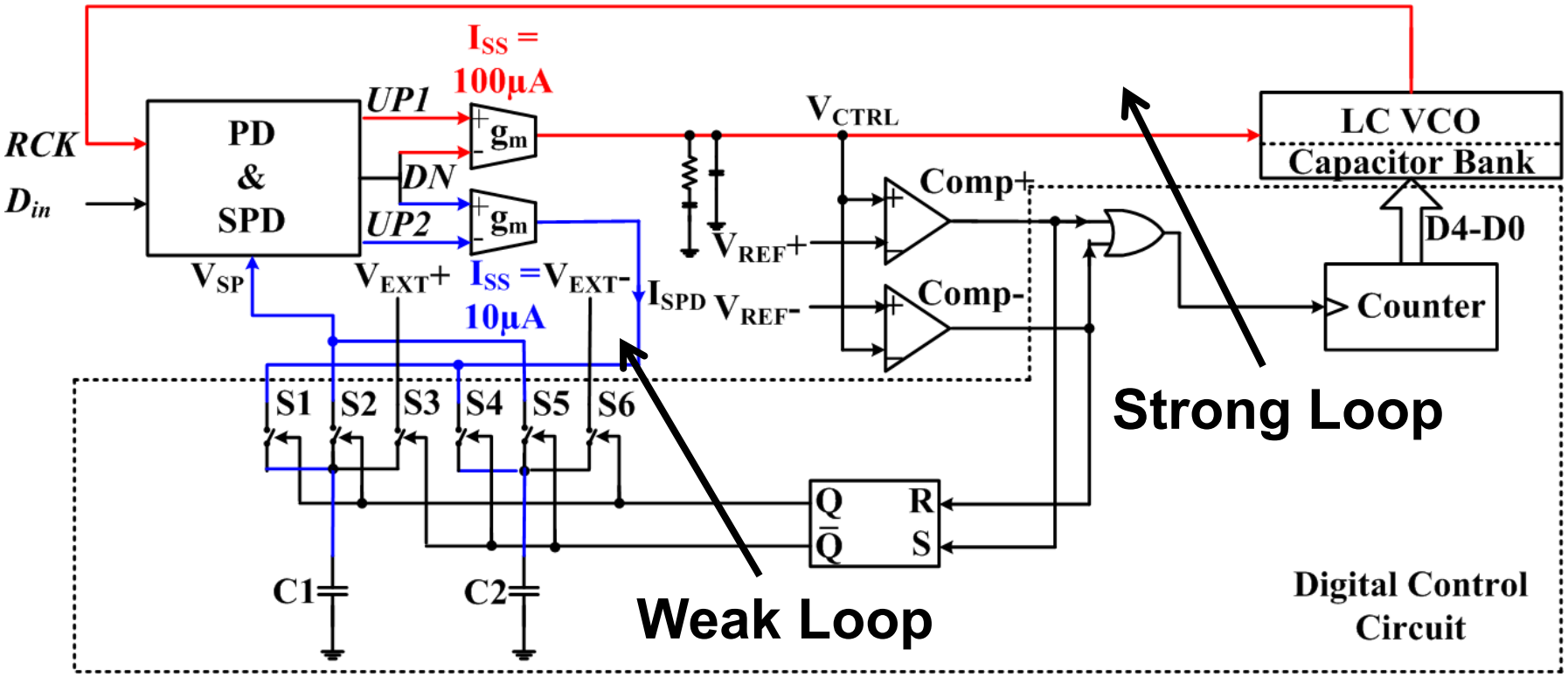


Linear Phase Detector Combined With Strobe Point Detector



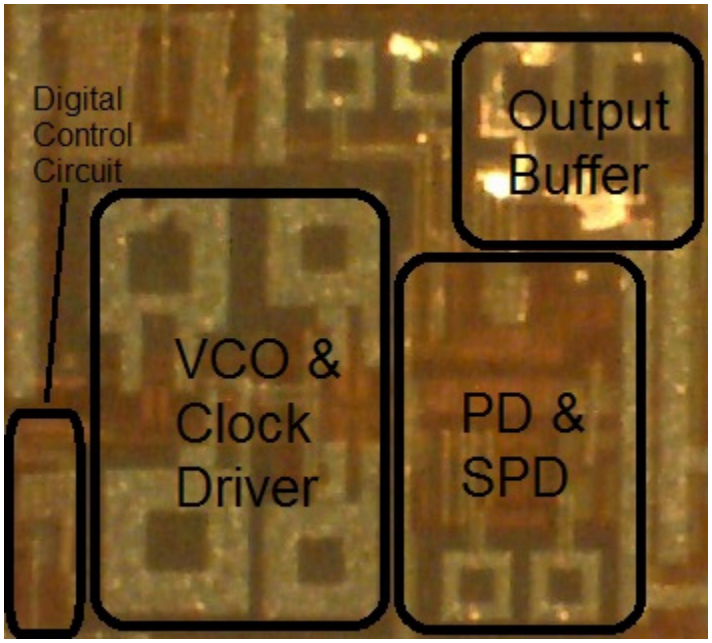
- DFF1, DFF2, and XOR2 are shared to reduce power dissipation.

FAM + PAM



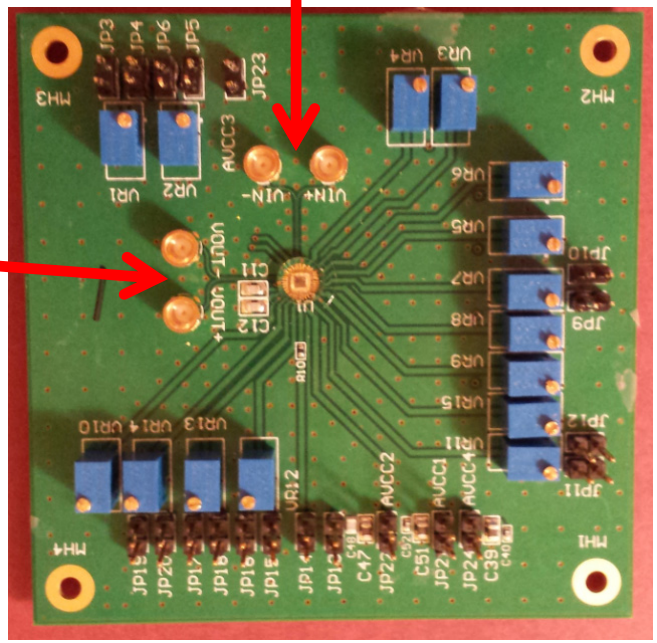
- Based on the magnitudes of the bias currents, the CDR loop is stronger than the phase adjustment loop.
- When the CDR loop is nearly locked, the phase adjustment loop dominates the behavior.

Test Chip & Board



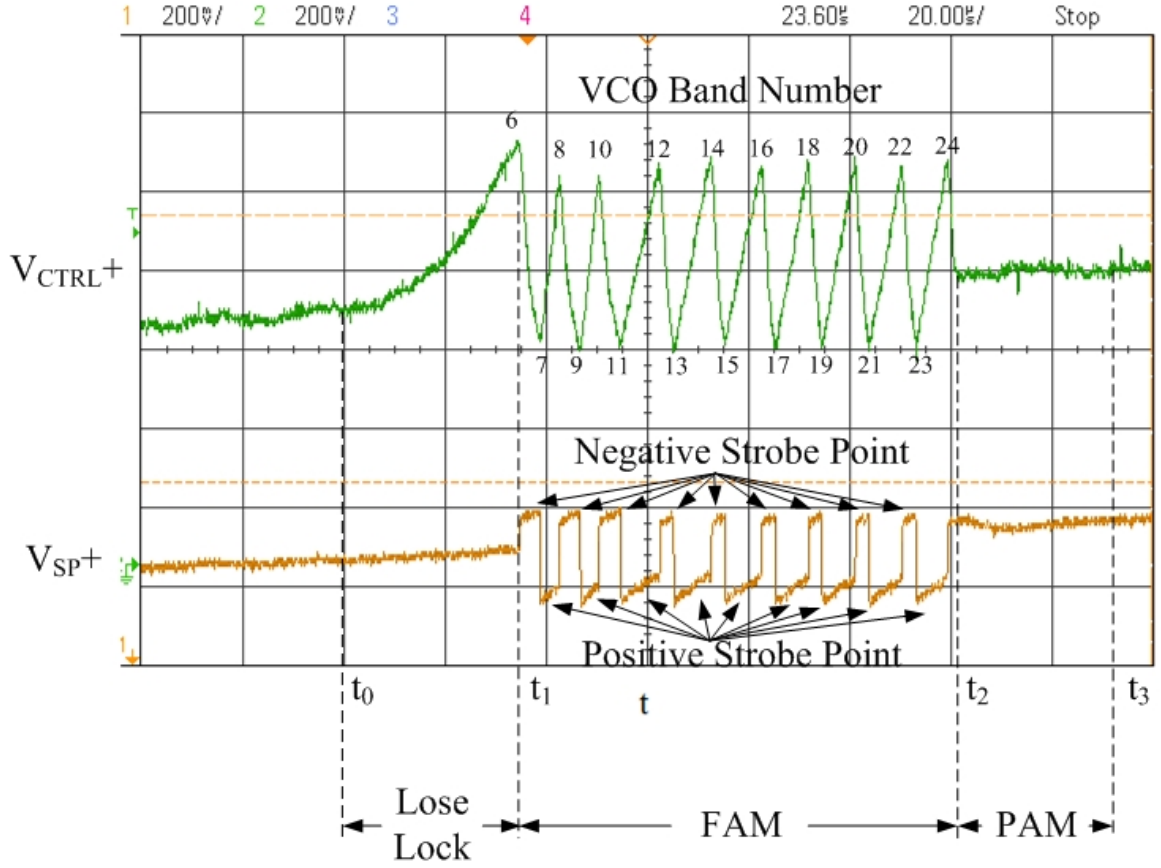
Differential Input

Differential
Output



- Chip fabricated using Jazz Semiconductor SBC18 0.18 µm BiCMOS technology. (Only CMOS transistors were used)
- The power supply voltage is 1.8 V, and the total power dissipation is 174 mW, not including the output buffer.

Frequency Acquisition Process

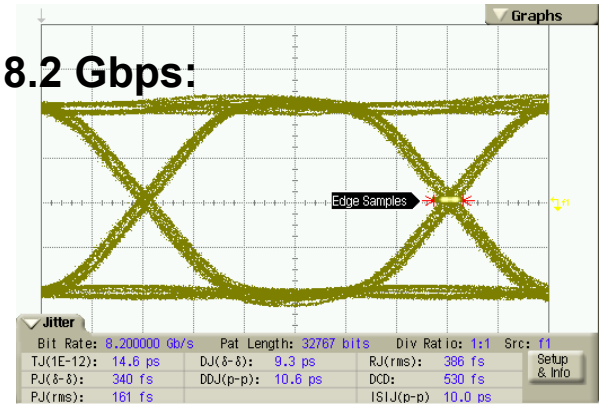


At t_0 the input bit rate is changed from 9.7 Gbps to 8.4 Gbps, and the CDR loses lock. At t_1 the CDR enters FAM. After sweeping 18 bands, the CDR enters PAM, and becomes stable at t_3. The total acquisition time is 116 µs.

Measurements

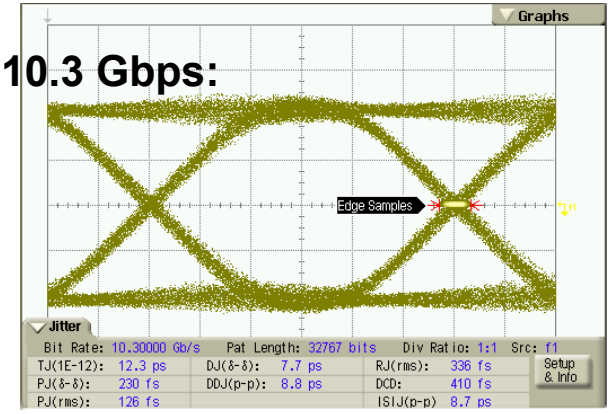
Eye Diagrams (2^{31}-1 PRBS):

8.2 Gbps:



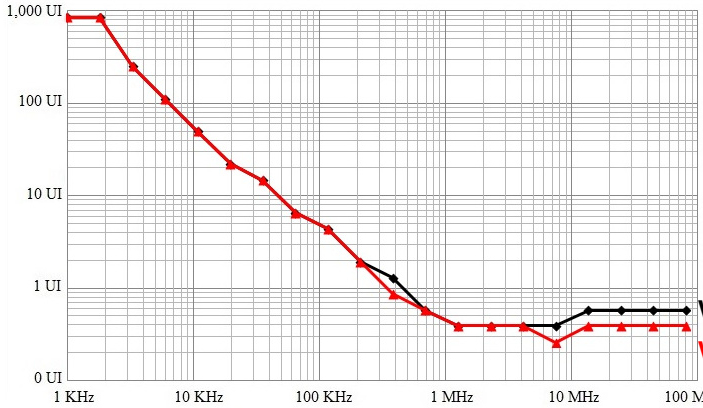
DJ = 9.3 ps p-p; RJ=0.386 ps rms

10.3 Gbps:



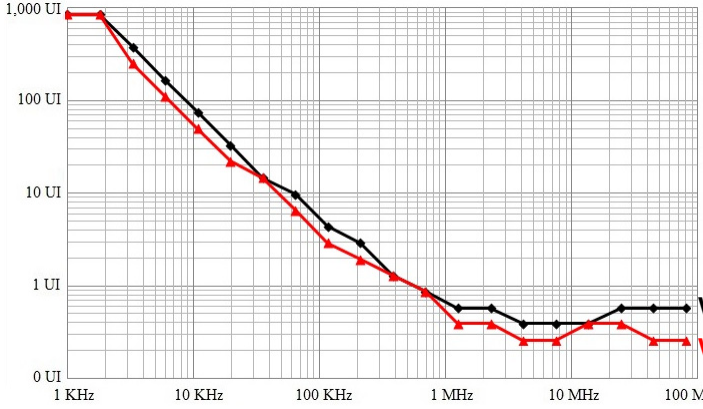
DJ = 7.7 ps p-p; RJ = 0.336 ps rms

Jitter Tolerance (2^{31}-1 PRBS):



with PAM, 0.58 UI
w/o PAM, 0.39 UI

8.2 Gbps



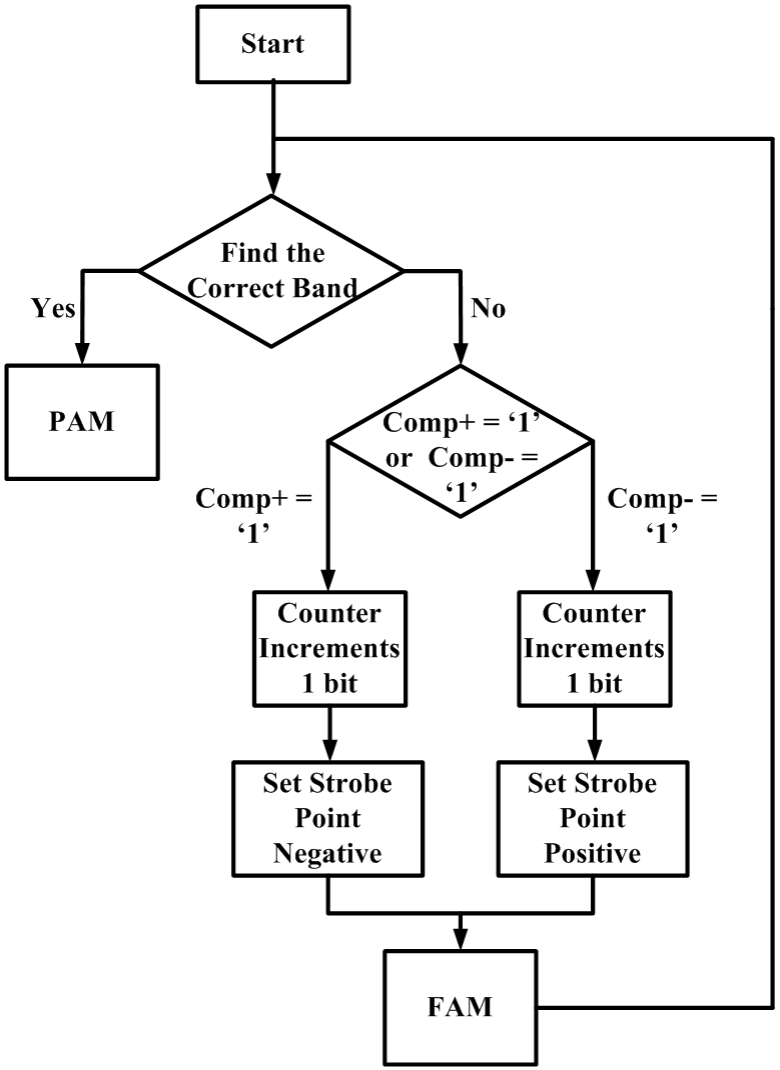
with PAM, 0.58 UI
w/o PAM, 0.25 UI

10.3 Gbps

Conclusions

- A linear phase detector used in a CDR can function as a frequency detector if the polarity of the strobe point is correctly selected based on the initial VCO frequency.
- The capture range of the designed CDR is from 8.2 Gbps to 10.3 Gbps with moderate power consumption.
- The robustness of the transition between frequency acquisition and phase locking is guaranteed.
- A strobe point adjustment mode is used to minimize the strobe point after locking.
- The rms random jitter and the peak-to-peak pattern-dependent deterministic jitter are 0.336 ps and 7.7 ps, respectively, at the 10.3 Gbps input bit rate with out-of-band jitter tolerance of 0.58 UI.

Appendix: Flow Chart of Referenceless CDR Architecture



A 40Gb/s VCSEL Over-Driving IC with Group-Delay-Tunable Pre-Emphasis for Optical Interconnection

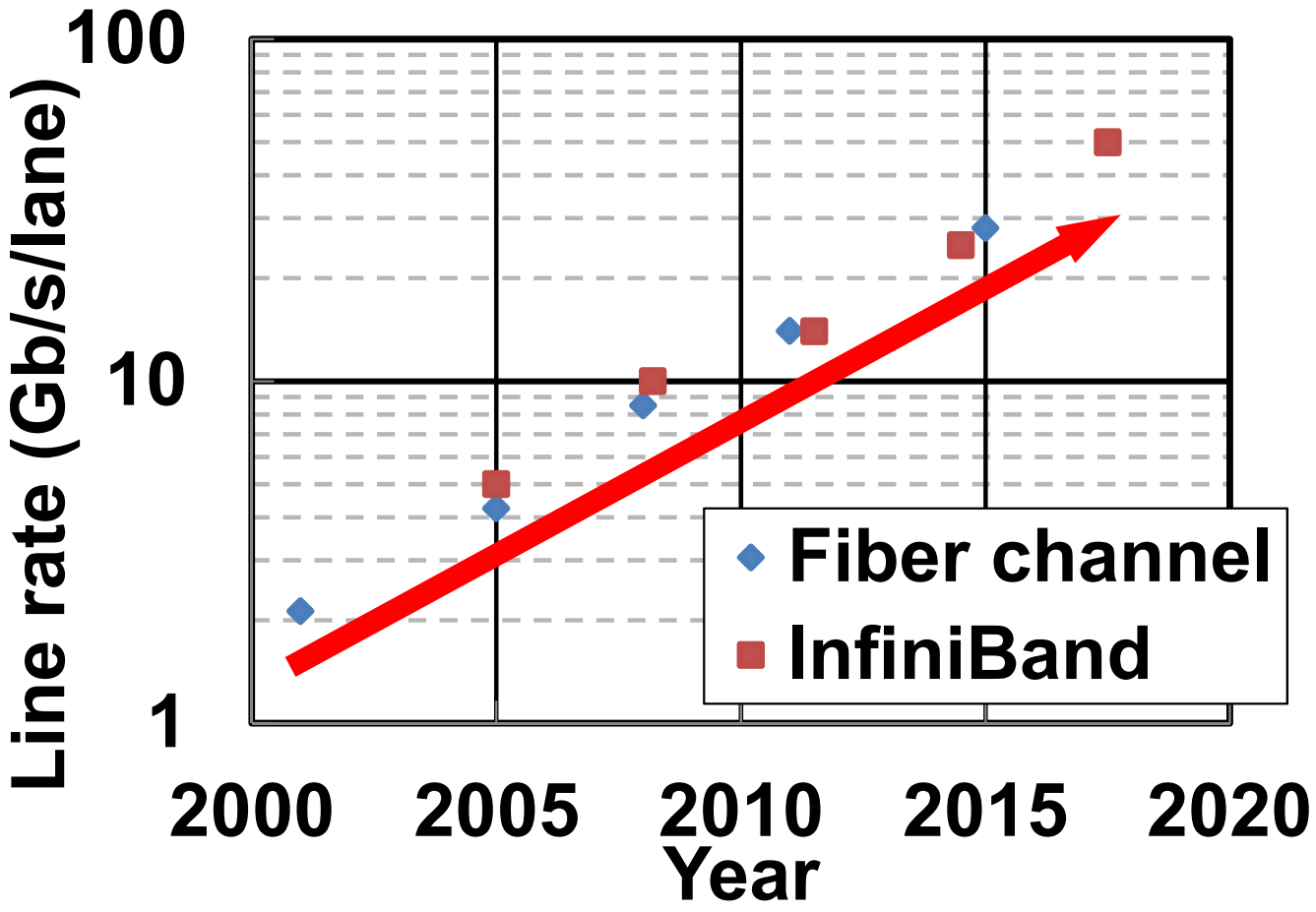
Yukito Tsunoda, Mariko Sugawara, Hideki Oku,
Satoshi Ide, and Kazuhiro Tanaka

Fujitsu Laboratories Ltd., Japan

Outline

- Motivation
- Design of 40Gb/s Optical Transmitter
  - High OMA output using group-delay compensation technology
  - Low power anode-driving output stage
- Measurement Results
- Summary

Data rate trend of interconnection



High-speed interconnection technology is developing

Next generation will be more than 25Gb/s/lane

High-speed interconnection transmitter

Requirements

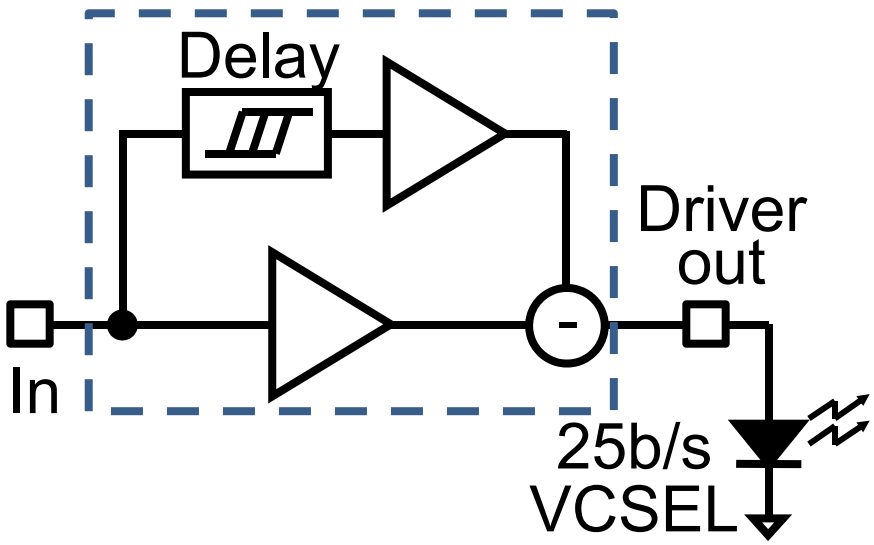
- High-speed VCSEL transmitter
  More than 25Gb/s/lane for next-generation
- Large Optical Modulation Amplitude (OMA)
  For long-distance transmission
- Low power
  For high-density interconnection

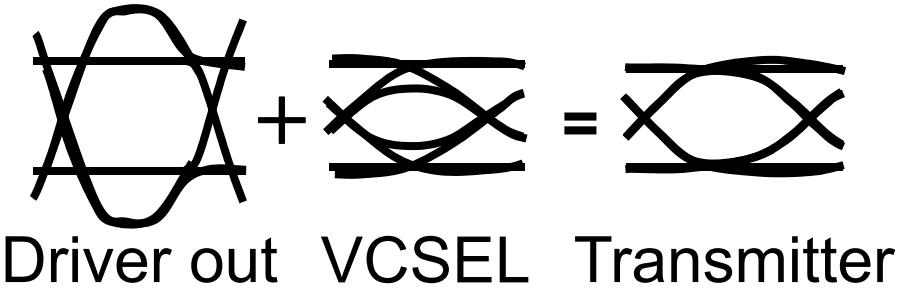
Approach

- 40Gb/s by over-driving with 25Gb/s VCSEL
- Anode-driving type output stage

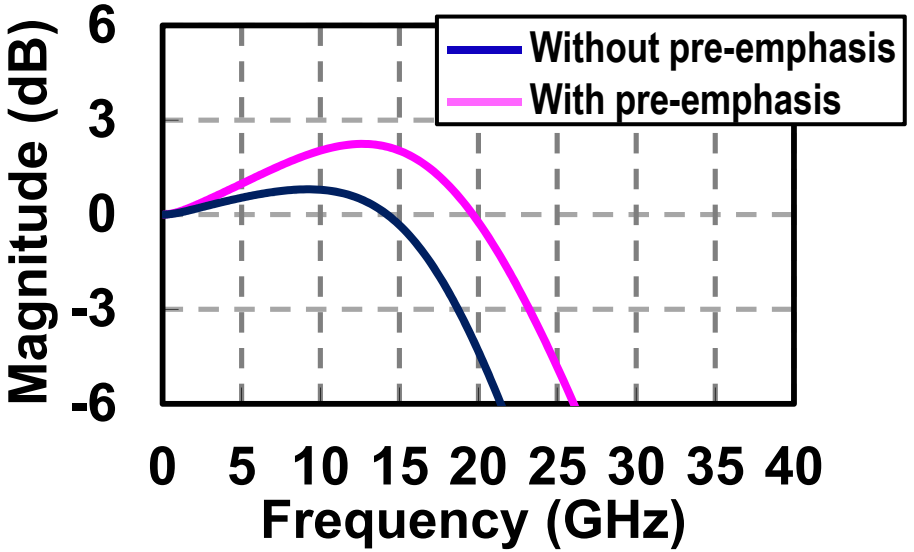
Over-driving VCSEL transmitter

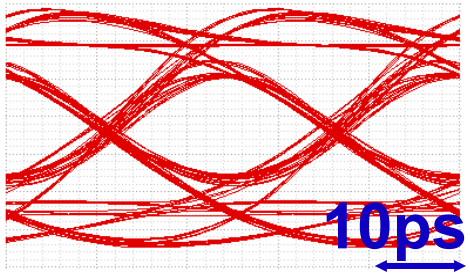
40Gb/s Transmitter



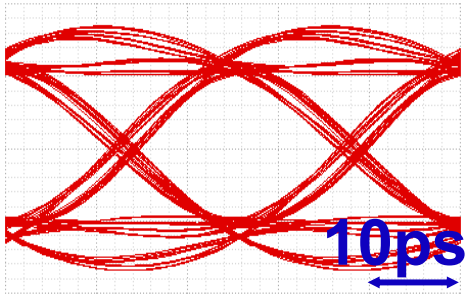


Transmitter output





Without Pre-emphasis

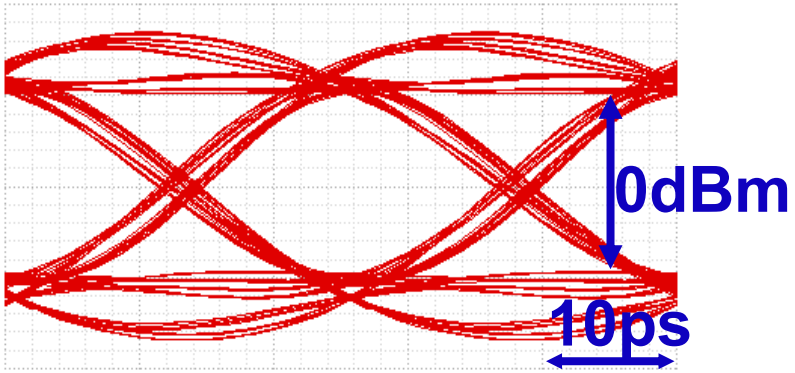


With Pre-emphasis

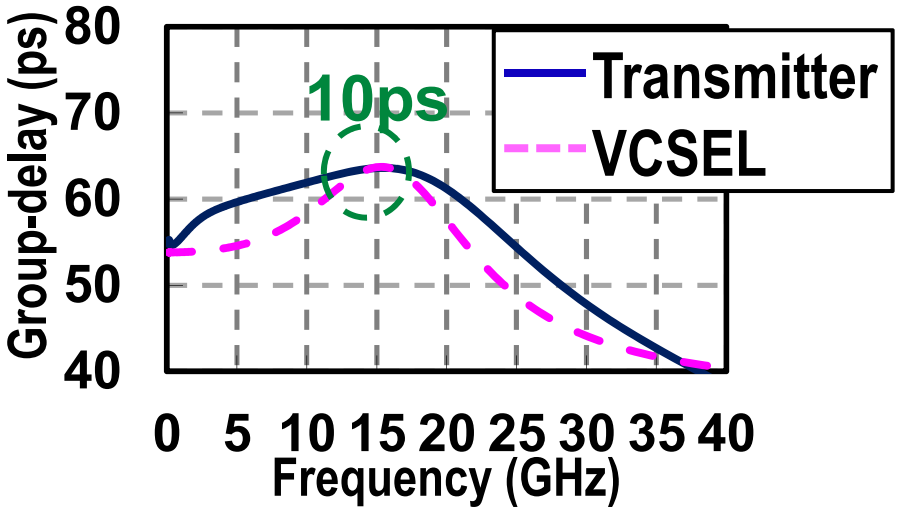
Over-drive VCSEL with pre-emphasis signal

Over-driving VCSEL transmitter issue

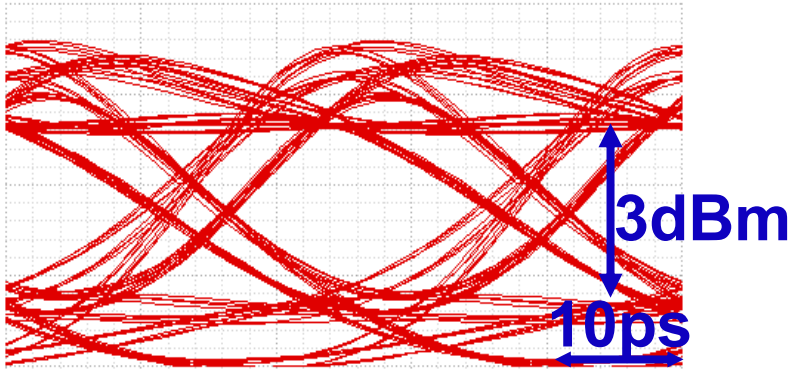
Low OMA (9mA bias, 0dBm out)



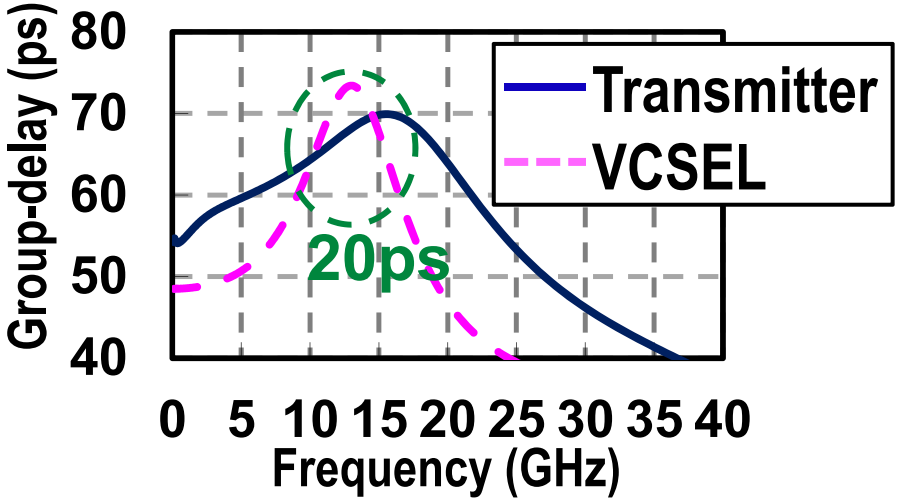
Transmitter out



High OMA (5mA bias, 3dBm out)

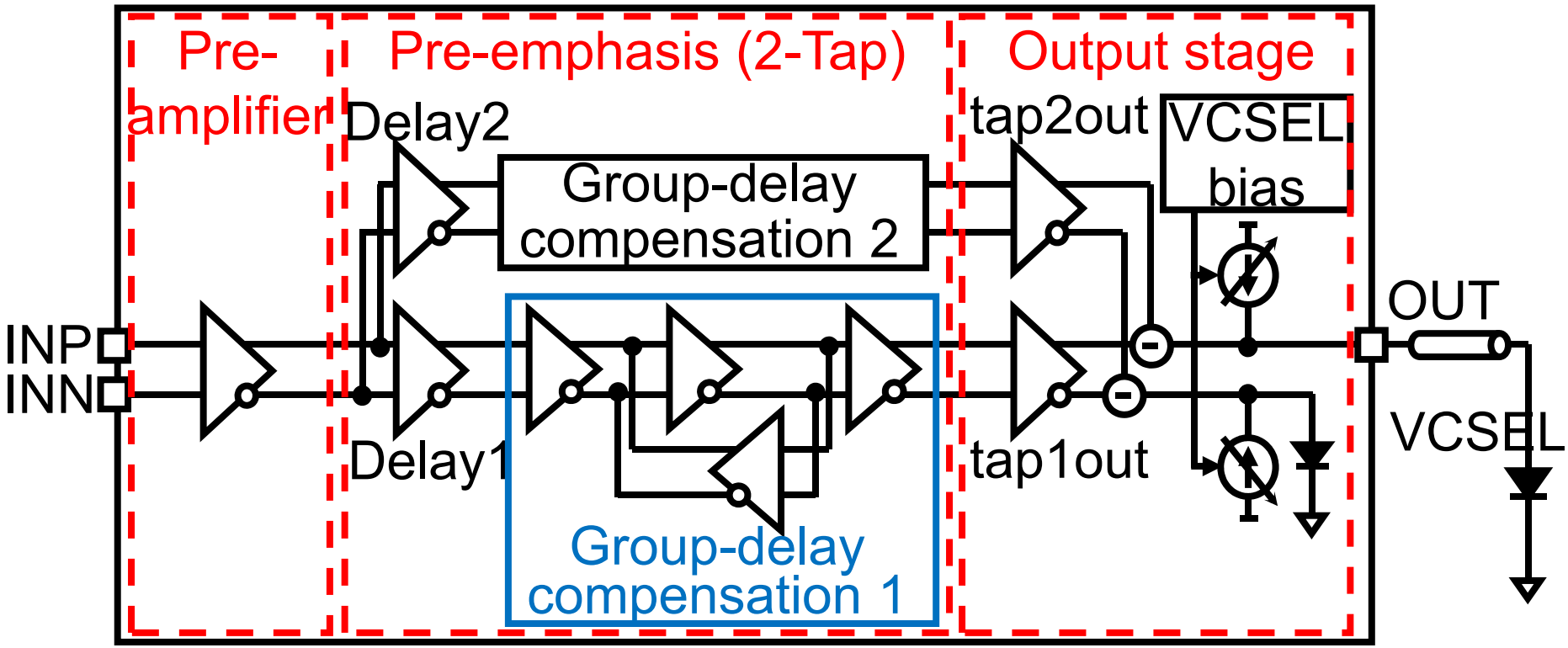


Transmitter out



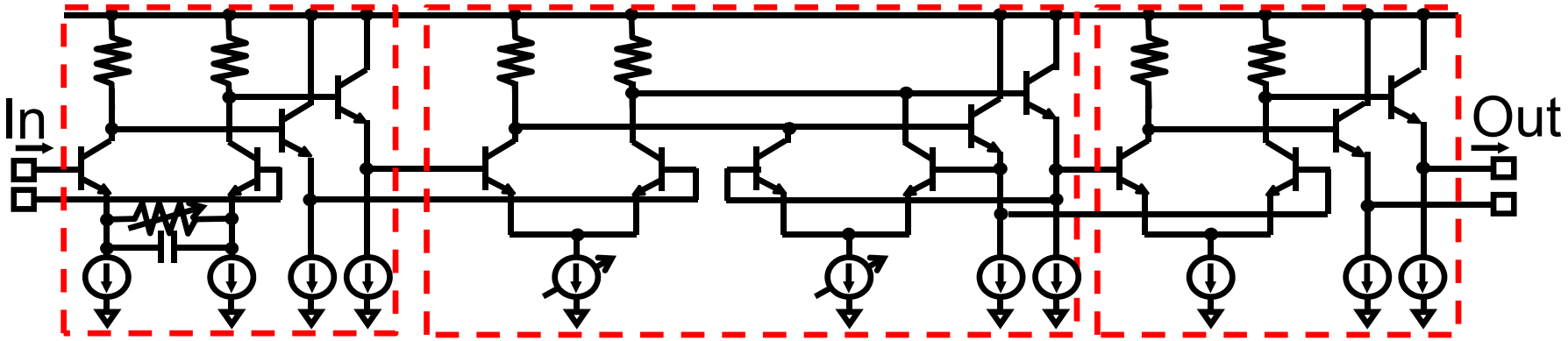
Large jitter was observed when the Tx output was 3dBm
Group-delay compensation is indispensable

VCSEL transmitter with group-delay compensation

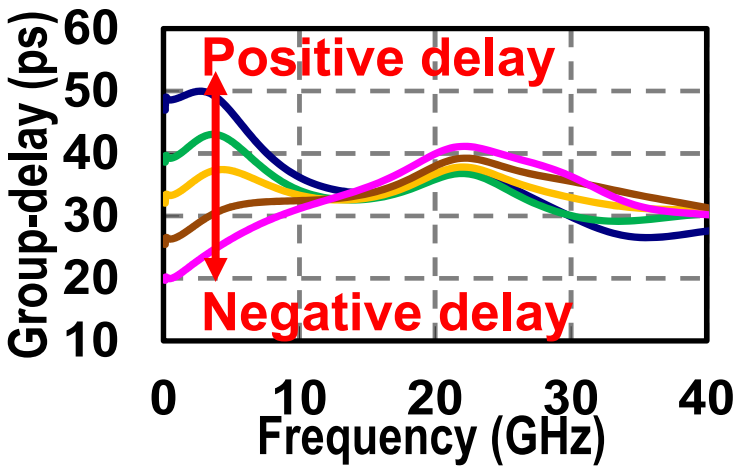


- 2-tap pre-emphasis with tap group-delay compensation
  - Reduce jitter caused by VCSEL characteristic
- Anode-driving type output stage

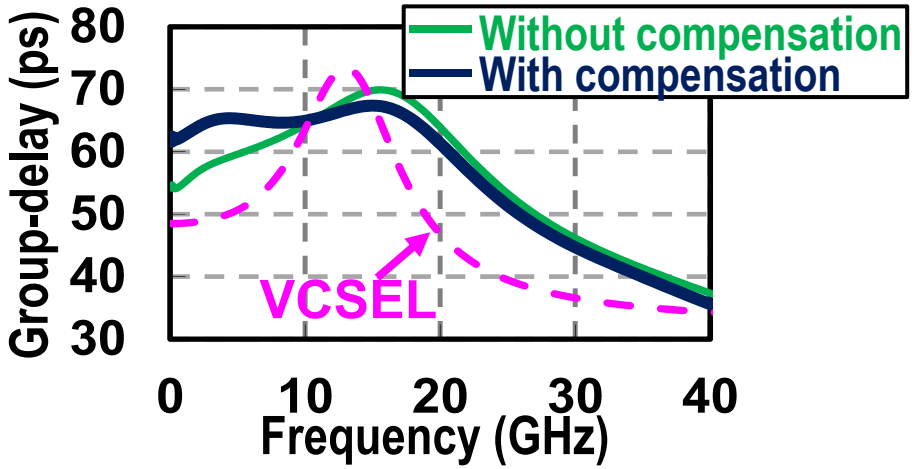
Group-delay compensation



Compensation circuit



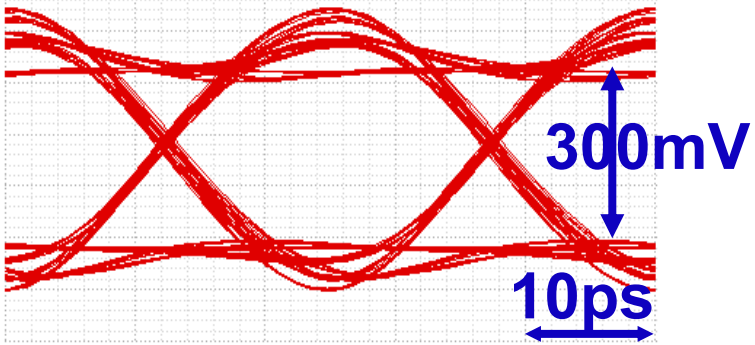
Pre-emphasis transmitter



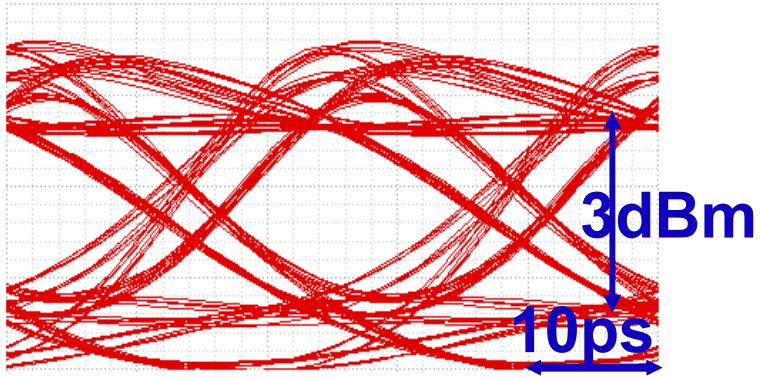
- Group-delay can be tuned by emitter peaking and positive-feedback
- Group-delay peaking of VCSEL can be compensated

Result of group-delay compensation

Without compensation

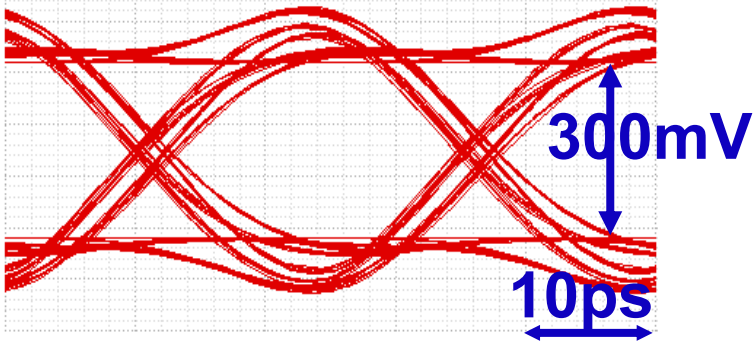


Driving waveform
(pre-emphasis)

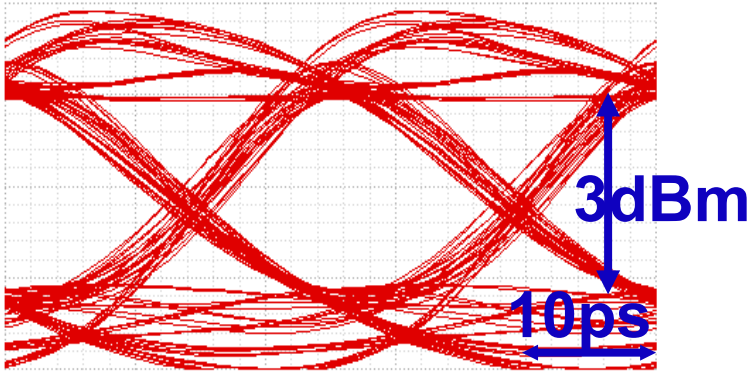


Pre-emphasis + VCSEL

With compensation



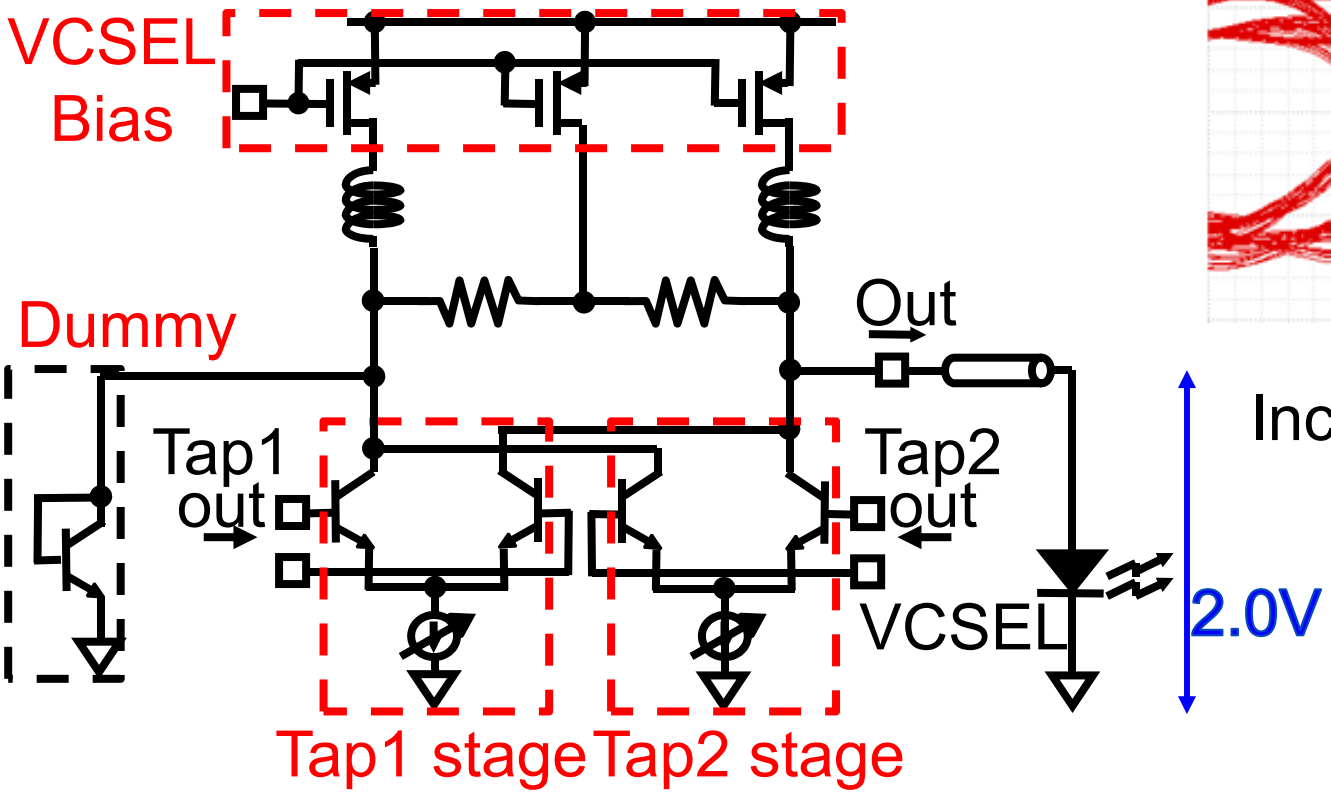
Driving waveform
(pre-emphasis)

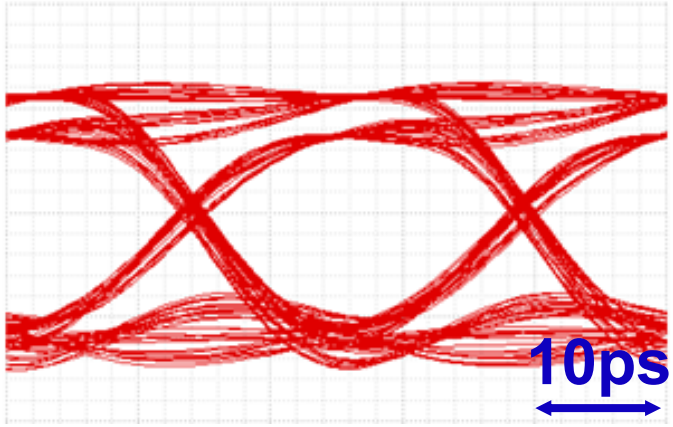


Pre-emphasis + VCSEL

Pre-jitter produced by group-delay compensation circuit improves VCSEL output

Anode-driving type output stage

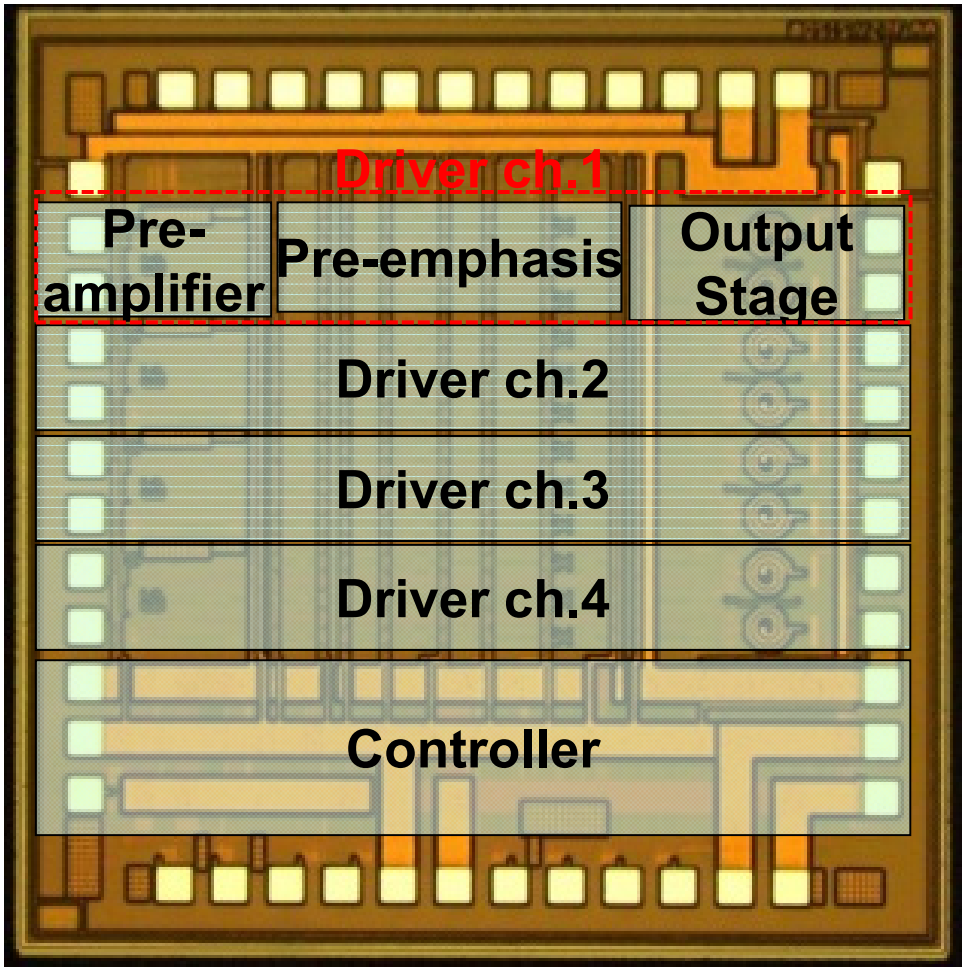




Driver output
Including output stage

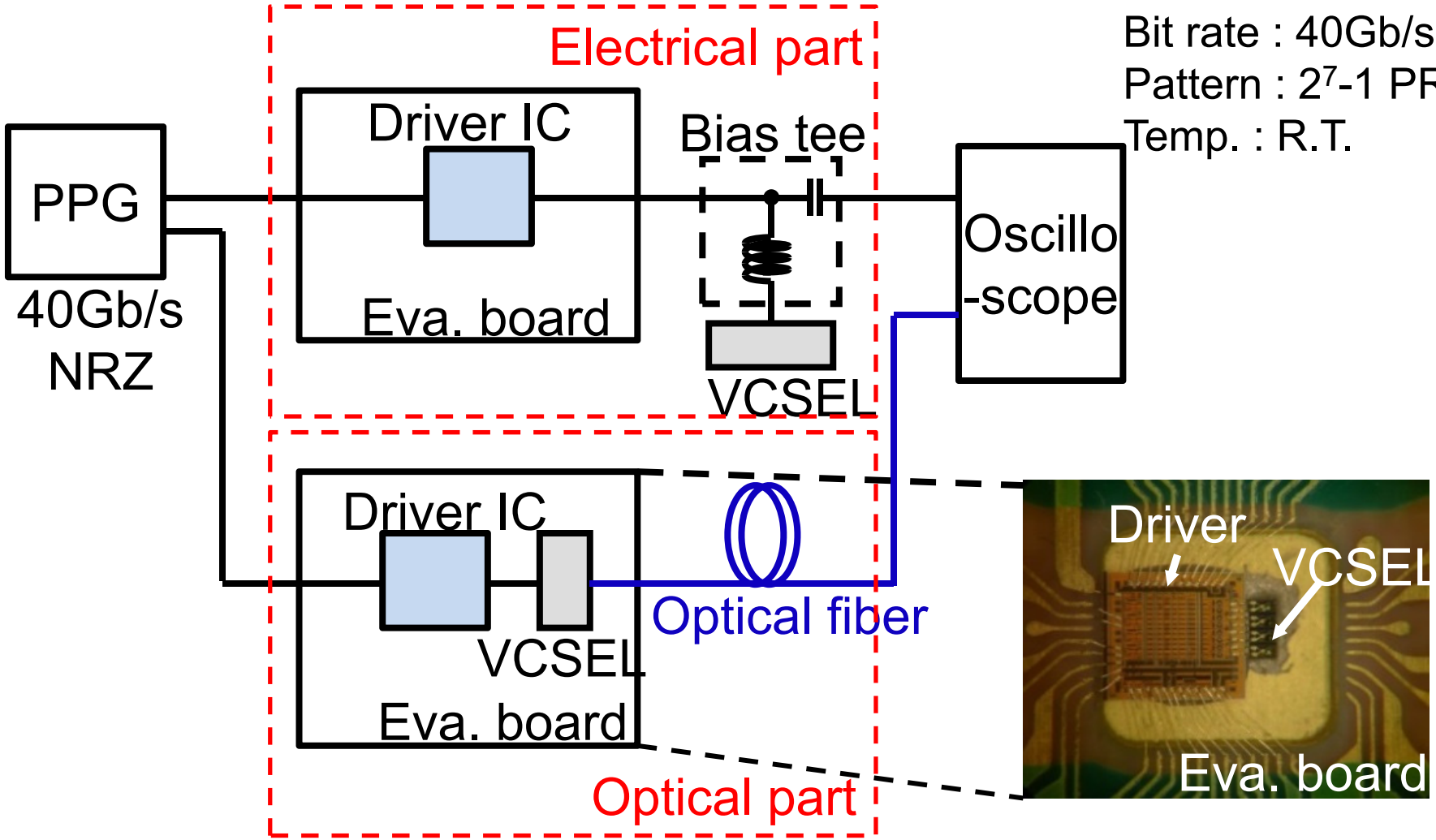
Anode-driving type output stage for low VCSEL supply voltage

Die layout



- 40Gb/s x4 over-driving VCSEL driver
- Fabricated in 0.13μm SiGe BiCMOS technology
- 2.0 x 2.0mm^2 (4ch + controller), 0.25 x 2.0mm^2/1ch

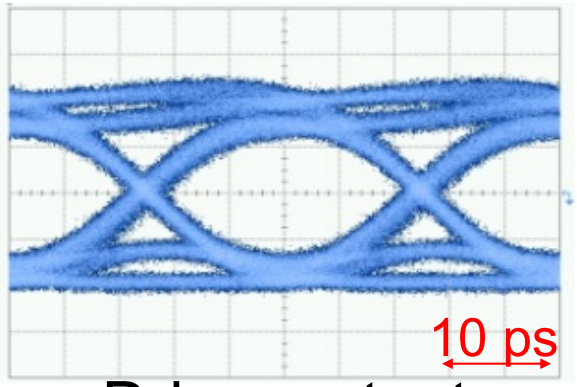
Measurement setup



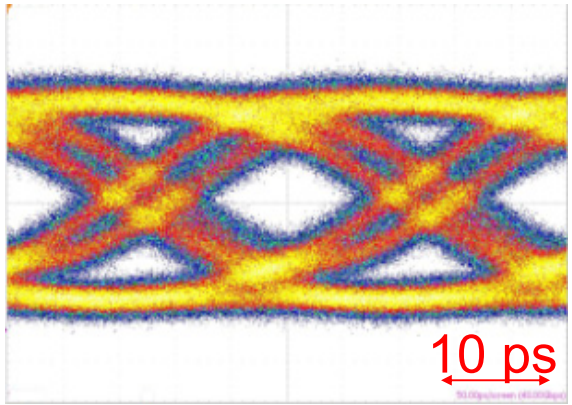
- Driver IC was evaluated using dummy VCSEL
- VCSEL output was coupled to optical fiber

Measurement result at 40Gb/s

Without pre-emphasis

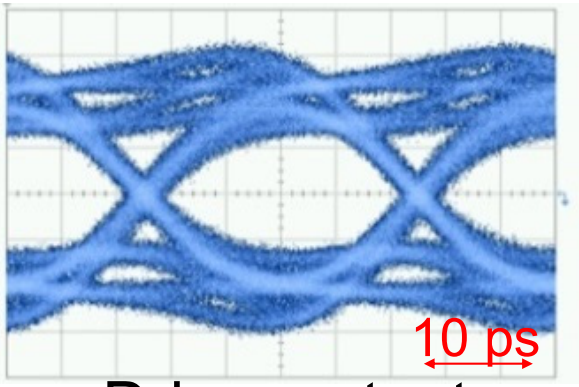


Driver output

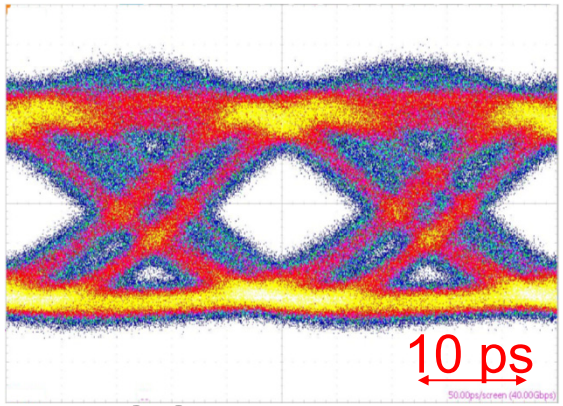


VCSEL output

With pre-emphasis

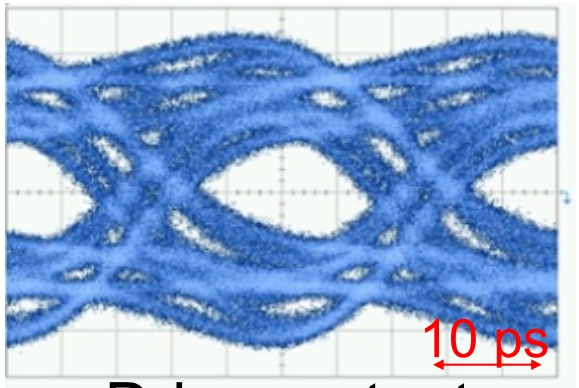


Driver output

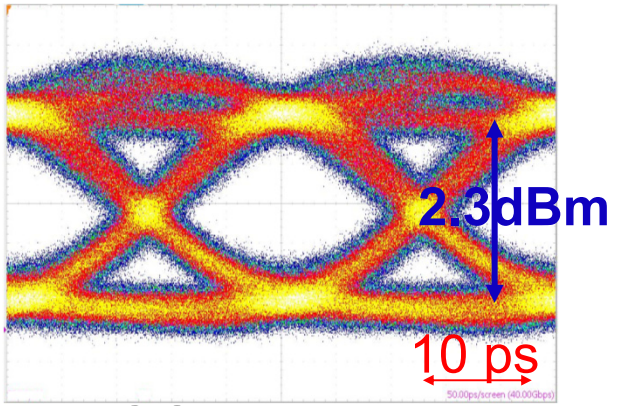


VCSEL output

With group-delay compensation



Driver output

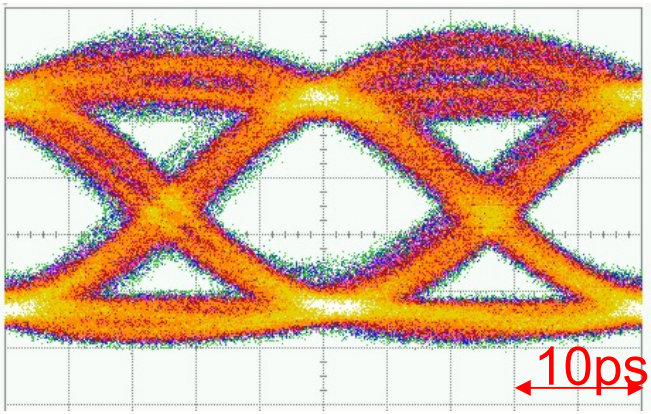


VCSEL output

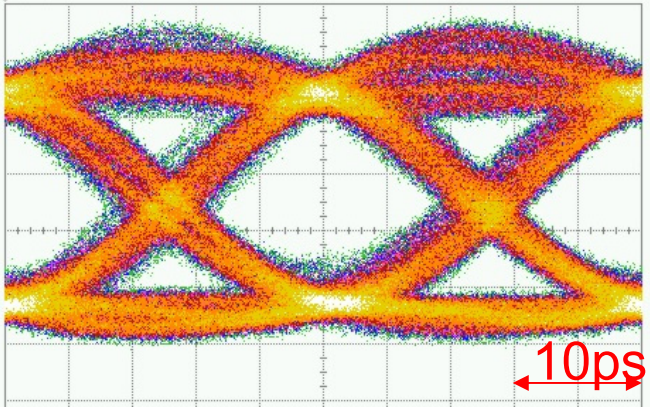
Pre-emphasis and group-delay compensation improves optical output

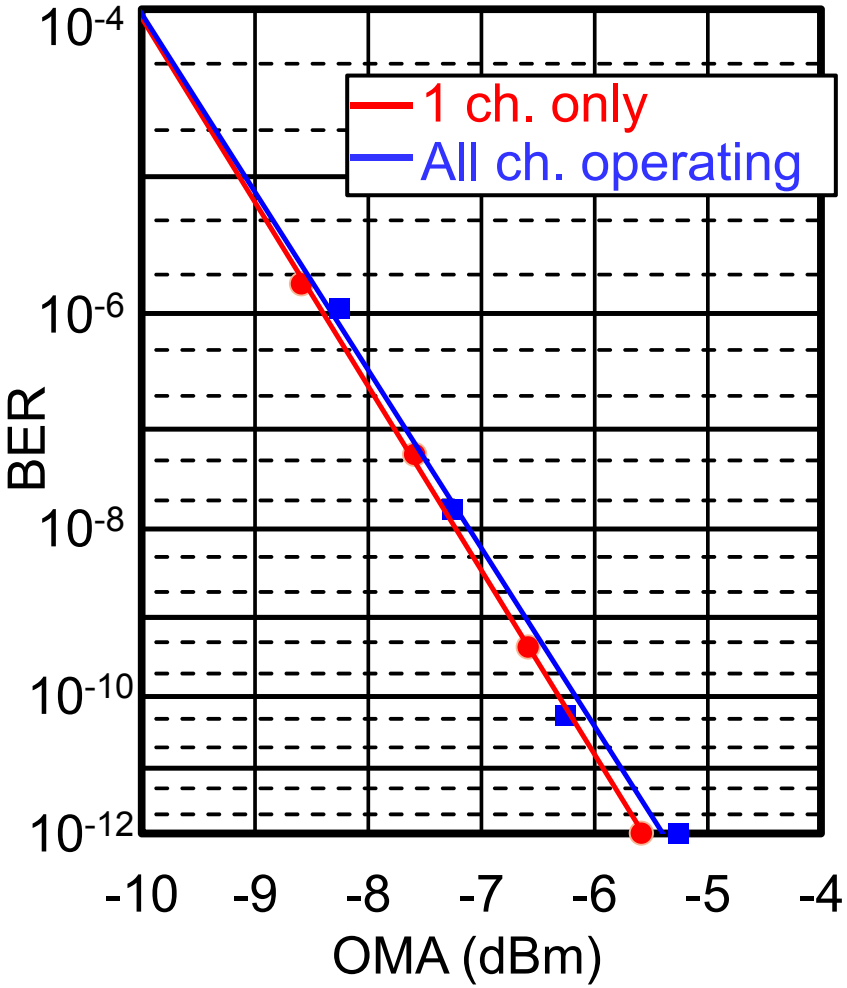
Performance with crosstalk

Optical output 1ch. only



Optical output all ch. operating





- Ch.2 was measured with and without ch.1,3,4 operating
- Error-free operation at 40Gb/s was observed
- Low crosstalk as 0.2dB

Performance summary

	[3]	[4]	[5]	This work
Technology	CMOS 65nm	SiGe 0.13μm	SiGe 0.13μm	SiGe 0.13μm
Data Rate (Gb/s)	25	40	56.1	40
Supply Voltage (V)	1.2/3.6	4.0/5.8	No data	2.5/3.3
Power Consumption (mW/ch)	99	530	682	312
Used VCSEL Bandwidth (GHz)	No data	16	24	16
Optical Modulation Amplitude (OMA) (dBm)	0.8	-1	No data	2.3
VCSEL Driver Type	Cathode Drive	Cathode Drive	Cathode Drive	Anode Drive

[3] J. Jiang et al., ISSCC2013
[4] A. Rylyakov et al., OFC2012
[5] D. Kuchta et al., OFC2013

Summary

- 2-tap pre-emphasis VCSEL driver with group-delay compensation
  - Compensates for group-delay of VCSEL
  - Double OMA with clear eye opening
- Anode-driving type differential output stage
  - Low power consumption
- Results of experiment
  - 2.3dBm OMA
  - 312mW/ch
  - Error free operation
  - Low channel crosstalk as 0.2dB